Critical Transient Processes of Enhancement-mode GaN HEMTs in High-efficiency and High-reliability Applications

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***Abstract*—Wide-bandgap devices, such as silicon-carbide metal-oxide-semiconductor field-effect transistors (MOSFETs) and gallium-nitride high electron mobility transistors (HEMTs), exhibit an excellent figure of merits compared to conventional silicon devices. Challenges of applying such fast switches include accurate extraction and optimization of parasitics especially when 6high-efficiency operation, all of which require the comprehensive understanding of such switch especially its interaction with peripheral circuits. Particularly for the enhancement-mode GaN HEMTs without the intrinsic body diode, when reverse conducting, its high voltage drop causes a high dead-time loss, which has rarely a concern in silicon devices. This paper focuses on 650V/30~60A enhancement-mode GaN HEMTs provided by GaN Systems, analytically models its switching behaviors, summarizes the impact of parasitics and dead time, and applies it in two DC/DC converters. Systematic design rules are generated not only for soft switching but also for hard switching applications.**

***Index Terms*—DC/DC converter, dead time, double pulse test, GaN HEMT, soft switching.**

I. Introduction

WIDE-BANDGAP (WBG) devices attract more and more attention in recent days as the promising alternative of Si devices. It is witnessed that in the past several years high-current GaN devices have been emerging quickly and applied in various power electronics applications, e.g., travel adapters, wireless chargers, smart home appliances, high efficiency AC-DC data-center power supplies, industrial motor drives and on-board EV battery chargers. Different from Si/SiC MOSFETs, GaN HEMTs are essentially hetero-junction devices, relying on the two-dimensional electron gas (2DEG) formed between GaN and AlGaN to conduct the current, shown as Fig.1. When imposing zero or negative voltage on the gate, the 2DEG will diminish thereby turning off the switch. Since electrons are travelling laterally between the drain and the source, the GaN HEMT is a typical lateral switch.

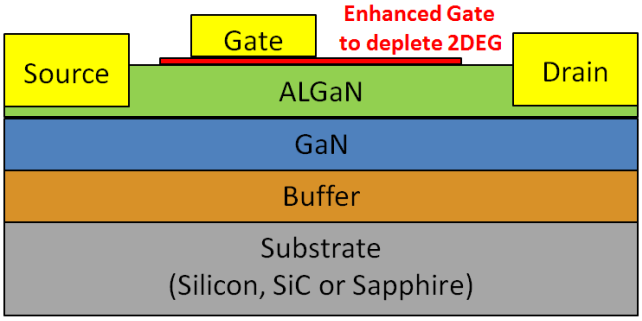

Fig. 1. Structure of E-mode GaN HEMTs.

Presently available GaN HEMTs are shown as Table.I. Among which, Transphorm and ON Semiconductor use the cascode design, i.e., employing a Si MOSFET to control of gate of the GaN JFET thereby forming a normally-off device. EPC; while Panasonic and GaN Systems use the enhancement-mode (E-mode) devices without any extra silicon gate. GaN Systems provides so-far the highest current rating of all GaN HEMTs, which is the study object of this paper.

TABLE I
POSSIBLE CANDIDATES OF GAN HEMTS

PartNumber	Manufacturer	V_{DS} /V	I_{ds} /A	R_{dson}/ mΩ	Package
GS66516T	GaN Systems	650	60	27	GaN *PX* 9x7.6x0.45
TPH3205WS	Transphorm	600	36	52	TO247
EPC2034	EPC	200	31	7	Passivated Die
PGA26E08BA	Panasonic	600	15	56	DFN 8x8 (BV-Typ)
NTP8G206N	ON Semiconductor	600	17	150	TO 220 Style 10
QFN8-HB2-1D	Sanken Electric	600	20	50	QFN 8x8x0.85 (mm)
AVJ199R06060A	Avogy	650		200	TO 220
MGG1T0617D	MicroGaN GmbH	600	30	170	Die

The impact of parasitics on a single device has been thoroughly discussed [1]-[4]. However, there is very little work focusing on the dynamic performance of paralleled GaN HEMTs [5]-[6], no mention paralleling more than 2 GaN HEMTs, which is thought to be extremely difficult [7]. Previous work is mainly focused on the inductance reduction

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[8]-[10] and loss modeling [11]. In addition, it is still recommended to adopt zero-voltage-switching (ZVS) technology to eliminate its switching-on loss to further enhance the efficiency. Such attempt has been implemented in [12], where a 7.2 kW on-board charger has been developed with >97% efficiency and ~4kW/L power density. Four GaN(GS66516T) have been paralleled to undertake 400V/92A hard switching-off reliably. Based on previous literatures, this paper aims to 1) further extend GaN application from the soft-switching to the hard-switching applications, given in some applications such as DC/AC inverters the hard switching is inevitable, and 2) realize more switch paralleling (>2) given that 60A is not enough for some high power applications. An analytical model to facilitate the understanding of switching process especially for paralleled GaN HEMTs is built in Section II. Based upon such model, in Section III a half-bridge power module with four paralleled GaN is designed. In Section IV, such devices/modules were experimented in two DC/DC converters as the design validation. Section V is the conclusion. The ultimate goal is to provide comprehensive understanding of such GaN devices, and more importantly, design criterion to ease the potential electrical stress during the transient process.

II. Modelling Dynamic Behavior of Paralleled GaN HEMTs with Parasitics

Take GS66516T(650V/60A) as an example. Its I-V curve at different temperature is shown in Fig.2, indicating an obvious positive correlation between the channel resistance and the temperature. Such characteristics guarantee the current balancing among paralleled switches in the steady state.

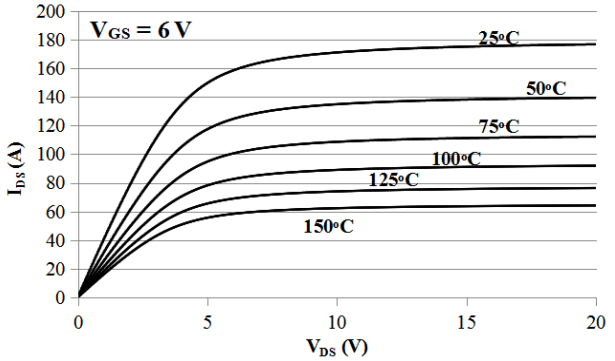


Fig. 2. V-I Curve of GS66516T vs. Temperature

The main challenge for the parallel operation, however, lies in the switching process, during which parasitics and gate driver circuits play critical roles. Different from most of Si MOSFET, E-mode GaN has relatively low turn-on gate-voltage threshold, e.g., ~2V, making it very sensitive to the high di/dt and dv/dt during the dynamic process. When V_{GS} exceeds 10V, such device will be destroyed. Therefore the electrical stress caused by parasitics need more attention than conventional Si devices. Any attempt of swapping Si with GaN without optimizing the circuit layout will result in the system failure.

In this section, we will first study two GaN HEMTs in parallel, locate potential influential factors and model their dynamic behaviors, which provides effective guidance for paralleling more GaN HEMTs in Section III. A half bridge consisting of two high-side and two low-side GaN HEMTs in parallel is shown as Fig.3, in which all parasitics are considered, and C2~C4 is the gate driver capacitors, C_{DC} is the decoupling capacitor, and R_{G1}~R_{G4} and R_{S1}~R_{S4} are the gate driver resistors.

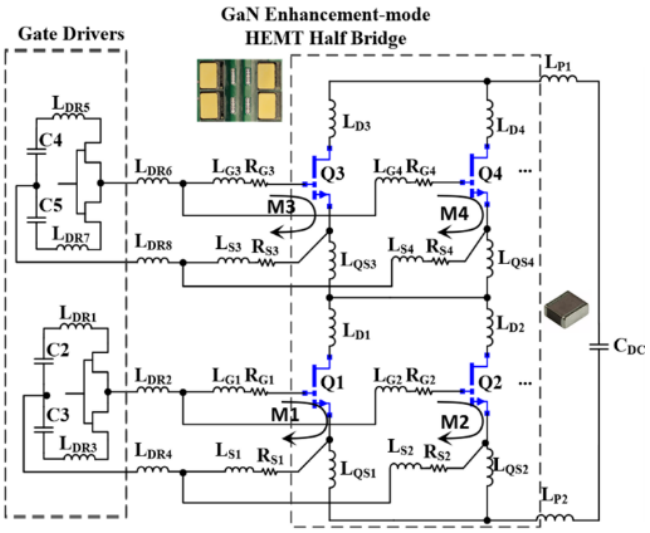


Fig.3. A Half Bridge with 2x GaN HEMTs in Parallel

Fig. 4a shows the switching-on process of paralleled GaN HEMTs. Here we divide the whole process into four intervals, i.e., P_1-delay period, P_2-*di/dt* period, P_3-*dv/dt* period and P_4-remaining switching period. Particular attention needs be paid to P_2 and P_3 since such periods bring the majority of current and voltage stresses to GaN HEMTs. Fig.4b shows the state trajectory of the switch during the turn-on process.

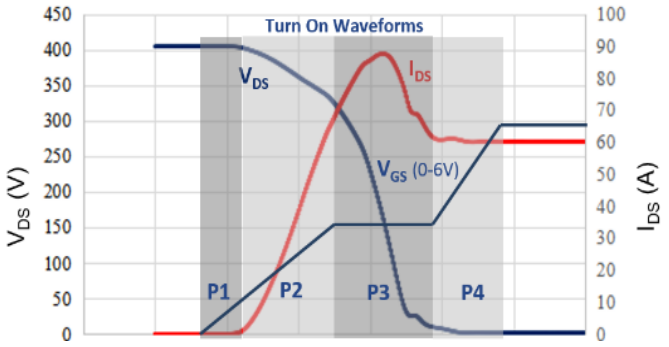


Fig. 4 (a). Vds, Ids Waveform During Switching on

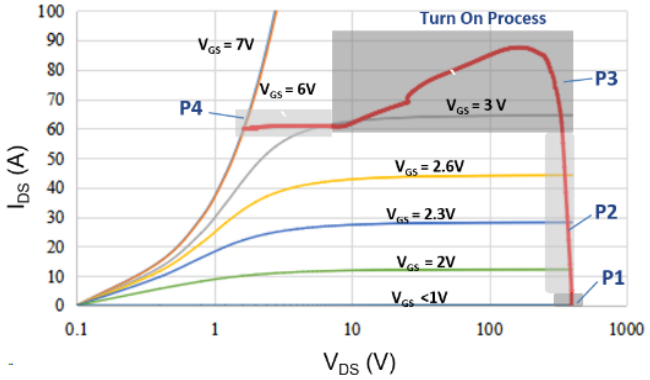


Fig. 4(b). State Transition of GaN HEMT During Switching on

P2: di/dt Period

After the gate-source voltage of any of paralleled HEMTs reaches the threshold, the impedance of 2DEG begins to decrease. In this mode, the HEMT is operated in the saturation region, drain current ($i_{D(t)}$) is controlled by gate-source voltage ($v_{GS(t)}$) i.e.,

$$i_{D(t)} = \mathrm{g} \cdot (v_{GS(t)} - V_{th}) \tag{1}$$

Here g is trans-conductance, and V_{th} is threshold voltage. As $v_{GS(t)}$ increases, $di_{D(t)}/dt$ starts to affect the gate voltage through the common-source inductance between gate-drive loops and power loops. To mitigate such cross talking, the Kelvin terminal is usually employed to bypass the common source inductance, as shown in Fig.3. Even so, such interaction between the gate and power loop has not fully resolved yet due to the existence of the quasi-common-source inductance (L_{QS_1} and L_{QS_2} as shown in Fig.5). The imbalanced quasi-common source inductance and high di/dt together will eventually cause a feedback voltage across gate source voltage as shown in (2). Such feedback voltage is regarded as the disturbance on gates of paralleled switches, which will be minimized if the layout is optimized ($L_{\mathrm{QS}_1} \approx L_{\mathrm{QS}_2}$) and current is evenly distributed among switches ($i_{D_1(t)} \approx i_{D_2(t)}$).

$$\boldsymbol{v_{QS_1(t)} = (L_{QS_1} \cdot \frac{di_{D_1(t)}}{dt} - L_{QS_2} \cdot \frac{di_{D_2(t)}}{dt}) \cdot \frac{Z_{s_1}}{Z_{s_1}+Z_{s_2}}} \tag{2}$$

Here, $v_{QS_1(t)}$ is the voltage across L_{S_1} and R_{S_1}, Z_{s_1} and Z_{s_2} are the impedance of L_{S_1}, R_{S_1} and L_{S_2}, R_{S_2} respectively.

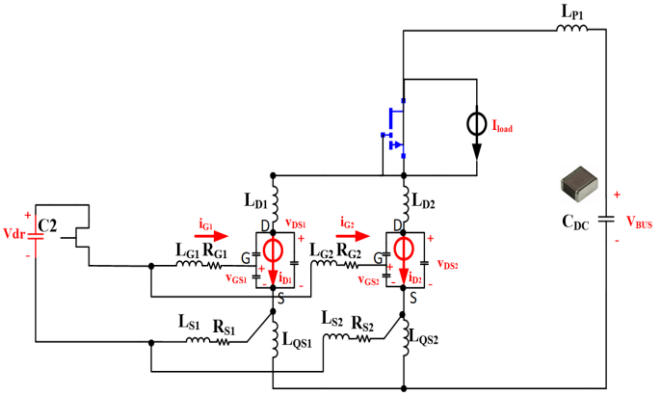


Fig. 5. Equivalent Circuit during di/dt Period of Switching on Process.

Based on KCL and KVL,

$$C_{GD_1} \cdot \frac{dv_{GS_1(t)}}{dt} + C_{GS_1} \cdot \frac{dv_{GS_1(t)}}{dt} = \frac{1}{R_{G_1}+R_{S_1}} (V_{dr} - v_{GS_1(t)} - v_{QS_1(t)} - M_1 \cdot \frac{di_{D_1(t)}}{dt} - (L_{G_1} + L_{S_1}) \cdot \frac{di_{G_1(t)}}{dt}) \tag{3}$$

$$v_{DS_1(t)} = V_{BUS} - L_P \cdot \left(\frac{di_{D_1(t)}}{dt} + \frac{di_{D_2(t)}}{dt}\right) - M_1 \cdot \frac{di_{G_1(t)}}{dt} - (\mathrm{L_{D_1}} + \mathrm{L_{QS_1}}) \cdot \frac{di_{D_1(t)}}{dt} \tag{4}$$

$$\mathrm{i_{G_1(t)}} = C_{ISS_1} \cdot \frac{dv_{GS_1(t)}}{dt} + C_{RSS_1} \cdot \frac{dv_{GD_1(t)}}{dt} \tag{5}$$

Here V_{dr} is the gate-drive voltage generated by the gate-drive ICs, M_1 is the mutual inductance between the gate-drive loop and power commutation loop,

P2 ends when $i_{D_1(t)}$ *or* $i_{D_2(t)}$ reaches I_{load}. Assuming $\frac{di_{D_1(t)}}{dt} = \frac{di_{D_2(t)}}{dt}$, v_{GS_1} is derived as (6).

$$v_{GS_1(t)} = V_{dr} + (V_{dr} - V_{th_1}) \cdot \left(\frac{s_2 \cdot e^{s_1 t} - s_1 \cdot e^{s_2 t}}{s_1 - s_2}\right) \tag{6}$$

Here $s_{1,2} = \frac{\pm\sqrt{b^2-4a}-b}{2a}$, $a = (R_{G_1} + R_{S_1}) \cdot C_{GD_1} \cdot \left(L_{D_1} + \frac{L_{P_1}}{2} + M_1 + L_{\mathrm{QS}_1} - L_{\mathrm{QS}_2}\right) + (C_{GS_1} + C_{GD_1}) \cdot (M_1 + L_{\mathrm{QS}_1} - L_{\mathrm{QS}_2} + L_{G_1} + L_{S_1})$, $b = 1 + \left(\mathrm{L_{QS_1}} - \mathrm{L_{QS_2}} + M_1\right) g + (R_{G_1} + R_{S_1}) \cdot (C_{GS_1} + C_{GD_1})$.

A higher gate driver voltage (V_{dr}) or smaller gate resistance ($R_G + R_S$) will lead to a faster switching transition, resulting in a lower loss.

Also, in this period, the quasi-common-source inductance (L_{QS_1}, L_{QS_2}) has a similar effect as the mutual inductance ($\mathrm{M_1}$), which might potentially cause overshoot or undamped ringing on v_{GS}. In [5] an unsynchronized gate-drive circuit is proposed, using one switch to fully turn on first before other switches. Its problem is that one switch undertakes majority of the turn-on current, which potentially lowers the system reliability. A symmetric power loop and gate driver loop layout is a better solution, as proposed and discussed in Section III to achieve the reliable switching.

P3: dv/dt Period

During this process, the impedance of 2DEG is controlled by gate-source voltage as shown in (7).

$$R_{2DEG} = \frac{v_{DS(t)}}{\mathrm{g} \cdot (v_{GS(t)} - V_{th})} \tag{7}$$

This period ends when $v_{ds(t)}$ reaches zero. The circuit behavior could be modelled as (8) & (9). Miller plateau is observed in this period during which $v_{GS_1(t)} = v_{GS_1\_miller}$.

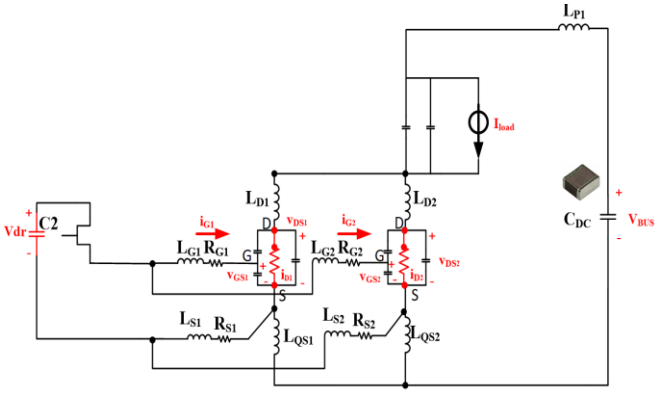


Fig. 6. Equivalent Circuit during dv/dt Period of Switching on Process.

$$C_{GD_1} \cdot \frac{dv_{DS_1(t)}}{dt} = \frac{1}{R_{G_1}+R_{S_1}} (V_{dr} - v_{GS_1\_miller} - v_{QS_1(t)} - M_1 \cdot \frac{di_{D_1(t)}}{dt} - (L_{G_1} + L_{S_1}) \cdot C_{GD_1} \cdot \frac{d^2 v_{DS_1(t)}}{dt^2}) \tag{8}$$

$$\left(I_{load} + C_{OSS_{total}} \cdot \frac{dv_{DS_1(t)}}{dt}\right) \cdot R_{2DEG} + L_{LOOP} \cdot C_{OSS_{total}} \cdot \frac{d^2 v_{DS_1(t)}}{dt^2} = V_{BUS} \tag{9}$$

Here $L_{LOOP} = L_{P1} + (L_{D1} + L_{QS_1})//(L_{D2} + L_{QS_2})$, $C_{oss_{total}}$ is the total output capacitance of both high-side and low-side transistors and R_{2DEG} is the 2DEG resistance of low-side transistors. So, $v_{DS_1(t)}$and $v_{GS_1(t)}$ of low-side HEMTs could be derived as (10) and (11).

$$v_{DS_1(t)} = V_{BUS} \cdot (1 - \frac{S_2}{S_2 - S_1} \cdot e^{S_1 \cdot t} + \frac{S_1}{S_2 - S_1} \cdot e^{S_2 \cdot t}) \quad (10)$$

$$v_{GS_1\_miller} = \frac{1}{R_1}(V_{dr} - (R_{G_1} + R_{S_1}) \cdot C_{GD_1} \cdot \frac{dv_{DS_1(t)}}{dt} - v_{QS_1(t)} - M_1 \cdot C_{GD_1} \cdot \frac{d^2 v_{DS_1(t)}}{dt^2} - (L_{G_1} + L_{S_1}) \cdot C_{GD_1} \cdot \frac{d^2 v_{DS_1(t)}}{dt^2}) \quad (11)$$

Here $v_{QS_1(t)}$ follows eqn (2), $s_{1,2} = \frac{\pm\sqrt{R_{2DEG}^2 - 4\frac{L_{LOOP}}{C_{OSS_{total}}}} - R_{2DEG}}{2 \cdot L_{LOOP}}$.

According to (7), the miller plateau voltage ($v_{GS_1\_miller}$) determines R_{2DEG} so as to control the slew rate of the drain-to-source voltage. From (7) to (10), the lower the miller plateau, the higher the channel resistance, therefore the longer time for V_{DS} to reach the steady state, representing the higher the switching-on loss. Meanwhile, according to (11), the larger the gate resistance, the lower $v_{GS_1\_miller}$, which results in a higher switching-on loss. Overall, (11) indicates that increasing the turn-on voltage or reducing the turn-on gate resistance is an effective solution to reduce the switching-on loss.

- *Switching-off Process*

The turn-off process is shown in Fig.7. Three intervals are included, i.e., P_1-delay period, P_2-dv/dt period, P_3-di/dt period.

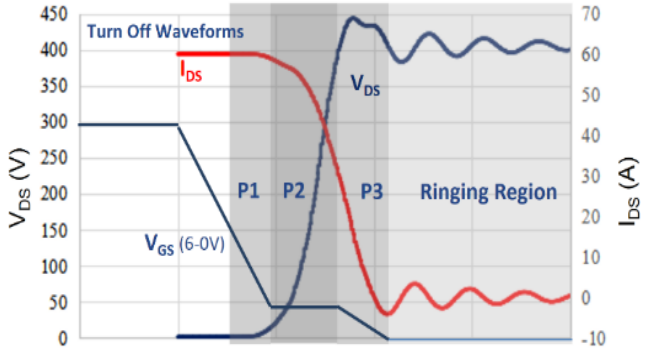


Fig. 7a. Waveform During the Switching-off.

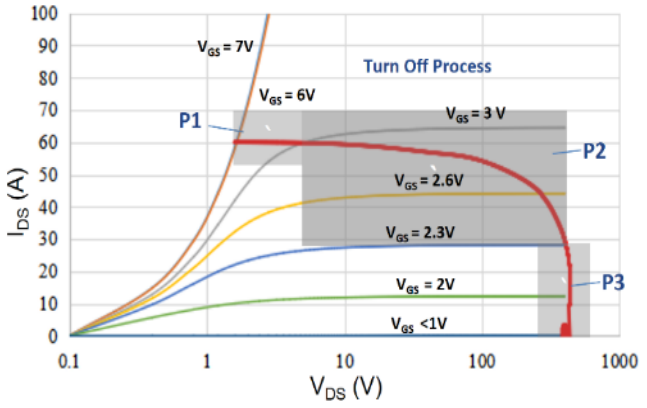


Fig. 7b. State Trajectory of GaN HEMT During the Switching-off.

P_2: dv/dt Period

Similar to *dv/dt Period* of switching on process, miller plateau will also be observed during this period. With the 2DEG impedance increasing, the load current (I_{load}) begins to discharge and charge high-side and low-side output capacitance, respectively. Here $C_{OSS_{total}}$ represents the overall output capacitance of the whole leg. $v_{DS_1(t)}$and $v_{GS_1(t)}$of the low-side HEMT are derived as

$$v_{DS_1(t)} = V_{BUS} \cdot (1 - e^{\frac{-t}{R_{2DEG} \cdot C_{OSS_{total}}}}) \quad (12)$$

$$v_{GS_1\_miller} = \frac{1}{R_1}(V_{dr\_off} + R_1 \cdot C_{GD_1} \cdot \frac{dv_{DS_1(t)}}{dt} + v_{QS_1(t)} + M_1 \cdot C_{GD_1} \cdot \frac{d^2 v_{DS_1(t)}}{dt^2} + L_1 \cdot C_{GD_1} \cdot \frac{d^2 v_{DS_1(t)}}{dt^2}) \quad (13)$$

According to (7), (12) and (13), the gate resistance determines the miller plateau voltage ($v_{GS_1\_miller}$) then further impacts the slew rate of the drain-to-source voltage. The larger the gate turn-off resistance, the lower $v_{GS_1\_miller}$. When the miller plateau voltage is lower than the threshold voltage, the 2DEG is pinched off. Adding a negative switching-off voltage, e.g., V_{dr_off}=-5V, expedites such switching process thereby reducing the switching loss. This period ends when the drain-source voltage reaches the bus voltage.

P3: di/dt Period

In this mode, the high-side transistors begin to freewheel the current. The low-side GaN HEMTs are shutting down. The $v_{GS_1(t)}$, $i_{D_1(t)}$,and $v_{DS_1(t)}$ is derived as (14), (15) and (16) assuming $\frac{di_{D_1(t)}}{dt} = \frac{di_{D_2(t)}}{dt}$.

$$v_{GS_1(t)} = V_{dr\_off} - (V_{dr\_off} - v_{GS_1 miller}) \cdot (\frac{s_2 \cdot e^{s_1 t} - s_1 \cdot e^{s_2 t}}{s_1 - s_2}) \quad (14)$$

$$i_{D_1(t)} = g \cdot (V_{dr\_off} - (V_{dr\_off} - v_{GS_1 miller}) \cdot (\frac{s_2 \cdot e^{s_1 t} - s_1 \cdot e^{s_2 t}}{s_1 - s_2}) - V_{th_1}) \quad (15)$$

$$v_{DS_1(t)} = V_{BUS} - L_{P_1} \cdot \left(\frac{di_{D_1(t)}}{dt} + \frac{di_{D_2(t)}}{dt}\right) - M_1 \cdot \frac{di_{G_1(t)}}{dt} - (L_{D_1} + L_{QS_1}) \cdot \frac{di_{D_1(t)}}{dt} \quad (16)$$

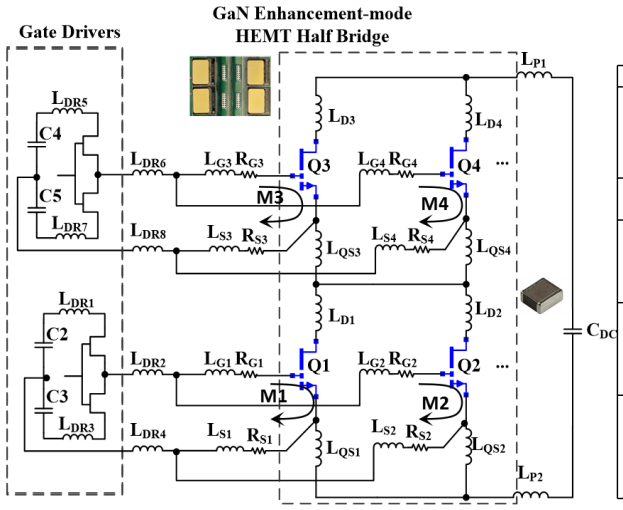
Here $s_{1,2} = \frac{\pm\sqrt{b^2 - 4a} - b}{2a}$, $a = (R_{G_1} + R_{S_1}) \cdot C_{GD_1} \cdot \left(L_{D_1} + \frac{L_{P_1}}{2} + M_1 + L_{QS_1} - L_{QS_2}\right) + (C_{GS_1} + C_{GD_1}) \cdot (M_1 + L_{QS_1} - L_{QS_2} + L_{G_1} + L_{S_1})$, $b = 1 + \left(L_{QS_1} - L_{QS_2} + M_1\right) g + (R_{G_1} + R_{S_1}) \cdot (C_{GS_1} + C_{GD_1})$.

Very similar to the di/dt period of switching on process, a higher gate driver voltage (V_{dr}) or smaller gate resistance ($R_G + R_S$) will lead to a faster switching transition, and the quasi-common-source inductance (L_{QS_1}, L_{QS_2}) has a similar effect as the mutual inductance (M_1). If 2DEG is shut off in P_2, P_3 does not exist.

- *Conclusion*

The paralleled GaN HEMTs' switching process is relatively complex. An analytical model in this section summarizes that the impact factors on switching performance, e.g., gate resistance, gate voltage and parasitics. More importantly, when in parallel, the quasi-common-source inductance and gate-to-power-loop mutual inductance introduce the cross talking between V_{DS} and V_{GS}. All these parameters need be optimized, which is shown in Section III.

The effects and design criterion of various parasitics existing in the gate-drive loop and power loop can be concluded as Fig.8.



Effects of Parasitics

Parameter	Description	Effect	Priority	Design Rules
L_{P1},L_{P2} L_{D1-4}	Commutation Loop Inductance	Increase Vds spike during P3 of Switching off	High	Smaller the better
L_{DR1}-L_{DR8}	Gate drive loop inductance	Increase Vgs ringing and overshoot	Medium	Smaller the better
L_{G1}-L_{G4} L_{S1}-L_{S4}		1. Increase Vgs ringing and overshoot, 2. susceptible to gate oscillation if very unbalanced	Medium	Smaller the better, as equal as possible for paralleled devices
M1-4	Mutual Inductance between power loop and gate loop	1.Feedback di/dt to Vgs, 2. Slowdown switching 3. potentially cause gate oscillation	Extremely High	
L_{QS1-6}	Quasi-common source inductance	1. Feedback the difference of di/dt to Vgs, 2. Balance current sharing 3. Potentially cause gate oscillation	Extremely High	

Fig. 8. Effects and Design Rules of Parasitic Parameters.

III. Construction of 650V/240A GaN Power Modules

A. Parasitics Optimization

The fast switching transition of GaN HEMTs results in a high *di/dt*, which further causes a voltage spike when coupled with the stray inductance in the power loop. Because of the extremely small input capacitance (C_{ISS}) of GaN HEMTs, a large gate-resistor sometimes is applied to slow down the switching transition thereby eliminating the voltage spike across the switch, which however increases the switching loss. To maximize GaN's advantage, minimizing the parasitic inductance is the ultimate solution.

The parasitic inductance is a function of the magnetic flux generated by current, as shown in (17).

$$L = \frac{\Psi}{I} = \frac{\int \dot{B} * d\dot{S}}{I} \tag{17}$$

A multi-layer PCB could significantly reduce parasitics of both the gate-drive loop and power loop by the magnetic-flux-canceling technique, i.e., the direction of the commutation current on two adjacent layers are opposite so that the generated flux outside the loop gets cancelled. Compared to the direct-bonded-copper (DBC) substrate, the PCB design could easily adopt the multi-layer structure with smaller loop area to achieve an excellent magnetic flux canceling effect.

A half-bridge power module consisting of four high-side and four low-side GaN HEMTs in parallel is shown in Fig.9a. Such model is rated at 650V/240A@25°C. The decoupling cap in located under the top and bottom switches to minimize the loop area, which in return reduces the loop inductance. On the other hand, the GaNPX™ package of such GaN Systems' devices with no leads or bonding wires, as shown in Fig.9b, also tremendously facilitates the parallel connections. Compared with traditional TO-247 package, the stray inductance is reduced by >80%.

Such a half bridge with four GaN HEMTs in parallel is modeled in ANSYS Q3D, and the power-loop and gate-drive-loop inductance are evaluated by Finite Element Analysis (FEA). The power-loop inductance of the proposed design is only 0.7 nH. For each paralleled GaN HEMT, its quasi-common source inductance is <0.2 nH, and the gate-drive-loop inductance is 4.2 nH. Effectiveness of such parasitics reduction will be verified later on the double-pulse tester (DPT).

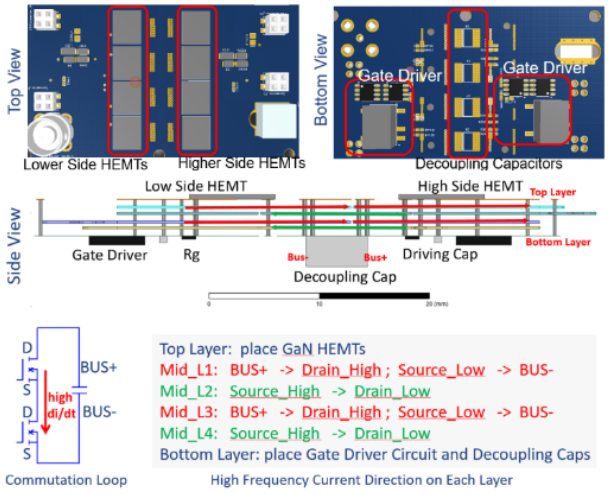


Fig. 9a. Layout of 650V/240A GaN HEMTs based Half Bridge.

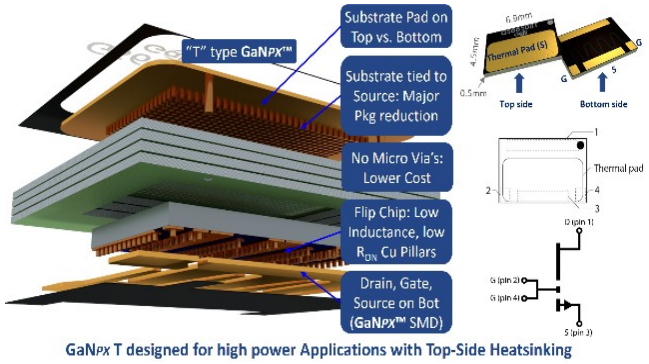


Fig. 9b. GaNpxTM Packaging.

B. Gate Driver Design

Candidates of the gate-drive circuit are shown in Fig.10. To mitigate the miller affect, a miller clamp circuit is proposed as Fig.10a. When the device is fully switched off, the miller clamping transistor is on to bypass the miller charge. Fig.10b is using different gate parameters to vary the switching-on/off speed. It requires two separate output terminals though. The gate-drive circuit in our system is shown in Fig.10c. Changing R_{on} and R_{off} will alter the switching on and off speed.

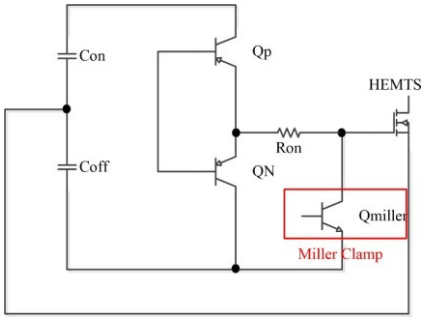


Fig. 10a. Miller Clamp Circuit.

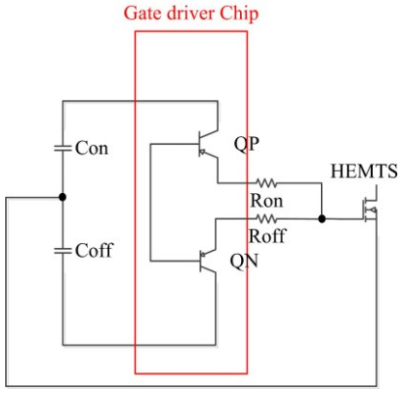


Fig. 10b. Two-gate-terminal Circuit.

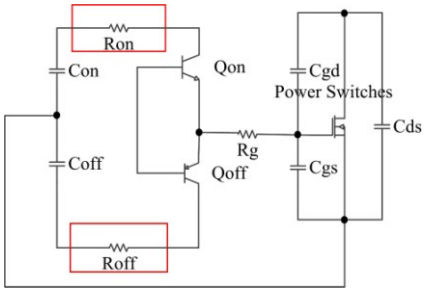


Fig. 10c. Gate-Drive Circuit used for GaN HEMTs.

Compared to other approaches, the gate-drive circuit shown in Fig.10c has the potential to integrate the gate-drive chip (Q_{on}, Q_{off} and R_g) with GaN devices on the same substrate, further reducing the gate-loop inductance. To vary the switching speed, only changing the two external resistors (R_{on} and R_{off}) is required, providing a very high flexibility.

C. Experimental Verification

A half bridge power module using four GaN HEMTs in parallel is shown in Fig.11a. Test carried out on the DPT at ~60A shows the perfect balancing between GaN HEMTs in both steady state and switching process, as shown in Fig.11b. This verifies the effectiveness of the gate-loop circuit design. We further pushed the turn-off current up to 240A, as shown in Fig.11c. The observed voltage spike is only 52V, validating the effectiveness of reducing the power-loop inductance.

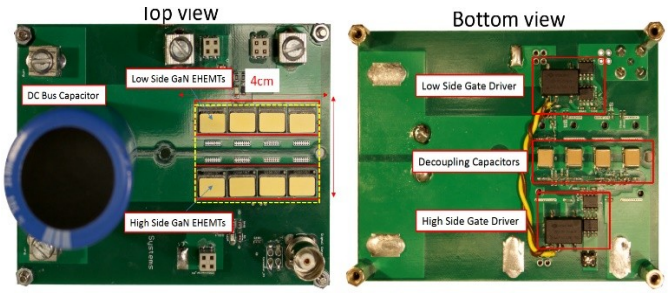


Fig. 11a. Prototype of 650V/240A GaN HEMTs based Half Bridge.

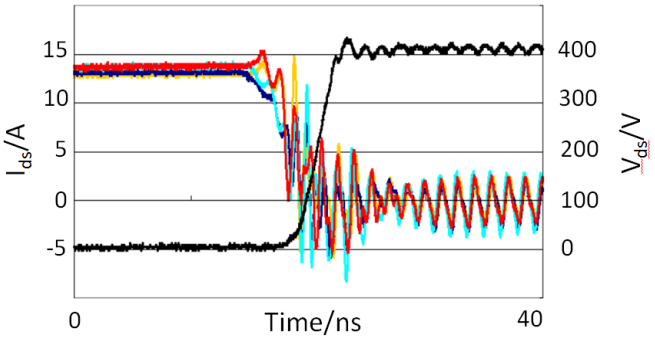


Fig. 11b. Current Balancing Among Four Paralelled Switches.

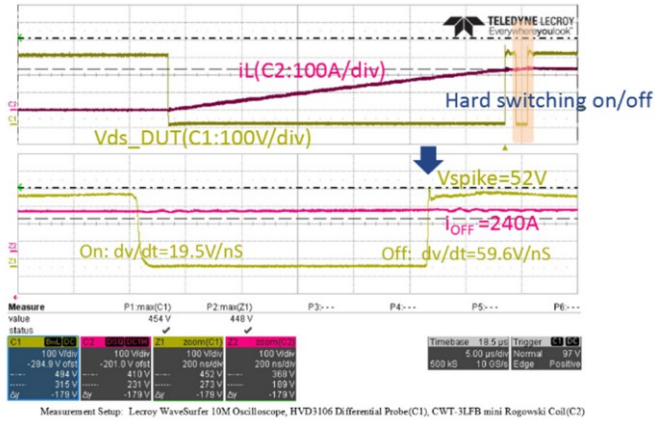


Fig. 11c. Double Pulse Test Waveform @400V/240 A.

IV. Applying GaN-HEMTs Power Modules in High-Efficiency Systems

The above effort is to minimize the harmful effect of parasitics. In this section, focus will be shifted to increasing the system efficiency. GaN HEMTs will be applied to two DC/DC converters, one is using the ZVS turn-on technique, the other is using the hard switching-on. Both converters adopt paralleled GaN HEMTs. The goal is to further investigate the interaction between GaN and peripheral circuits during the transient processes in the actual system.

A. Soft-switched DC/DC Converter

Even though GaN HEMTs have superior performance over Si devices, it still has much more switching-on loss than switching-off loss. When possible, ZVS turn-on is still preferred even when using GaN.

As shown in Fig.12, when switches in the same leg are both off, the energy stored in the external inductor begins to discharge C_1 and charge C_2. Here C_1 and C_2 are the switch output capacitance. Once C_1 is fully discharged, Switch_1 is ZVS on, resulting in no switching-on loss.

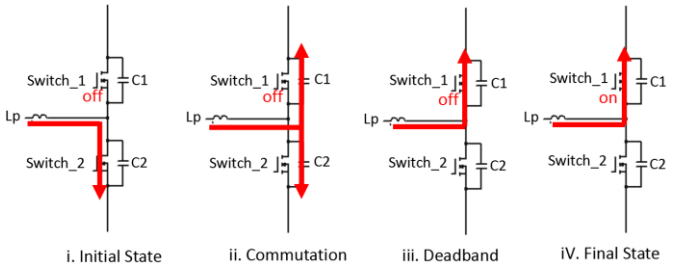


Fig. 12. Impact of Coss on Zero Voltage Switching Process.

To secure ZVS, the inductor current must be high enough to deplete the overall output capacitance (GaN HEMTs + PCB board) within the dead time. Determination of the dead time and minimum required load current requires an accurate extraction of parasitic capacitance. Note when placed on the PCB, parasitic capacitance introduced by the PCB and other components is not negligible, given that C_{oss} of the GaN HEMT is ultra small. Such parasitic capacitance could be extracted after modelling the whole PCB in ANSYS Q3D. More accurately, an experimental method using the DPT is preferred, shown as Fig.13a. The current spike measured during hard switching on lower switches is contributed by charging the output capacitance of top switches. The integral of such a spike current divided by the DC-bus voltage indicates that equivalent capacitance is about 2nF for top switches. Therefore, the overall capacitance of the whole H-bridge is 4nF. Note such method is only effective to GaN instead of Si/SiC. Since no body diode exists inside GaN HEMTs, such current spike is solely introduced by charging the C_{oss} without including the diode reverse-recovery current.

In the reverse conduction mode, the drain will behave as the source and the source will act as the drain. When V_{GD} is higher than $V_{th\_GS,}$ the switch turns on. The voltage drop across the switch is

$$V_{SD} = V_{th\_GD} - V_{GS\_off} + I_D * R_{DSon} \quad (18)$$

Since the gate threshold of GaN HEMTs is ~2V while a negative V_{GS_off} = -5.2V is added to reduce the switching loss, (18) indicates a voltage drop of ~7V in the reverse conducting mode, much larger than Si devices. A large dead time for GaN HEMTs will certainly result in the increment of the dead-band loss. On the other hand, if the dead time is too small, the switch will lose ZVS since no enough time is given to deplete the top-switch C_{oss}, as shown in Fig.12, which results in the increment of the switching-on loss.

One argument is the possibility to drop the dead-band loss by anti-paralleling a SiC Schottky diode to the GaN HEMT. Firstly, such an external diode will bring additional junction capacitance and introduces the reverse-recovery current in hard switching applications. An experimental comparison between w/n anti-parallel diode C3D10065A to GaN HEMTs is shown as Fig.14. Obviously adding an anti-paralleled diode will result in the significant increment of the switching-on loss, unless the ZVS turn-on is adopted.

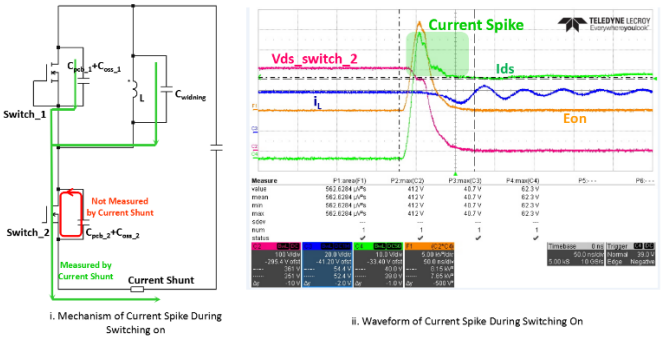


Fig. 13a. Current Spike Measurement with Double Pulse Test Platform.

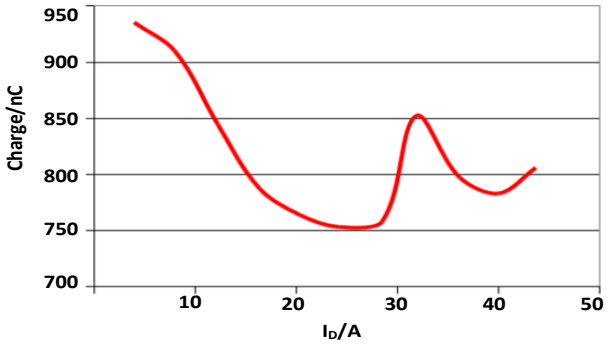


Fig. 13b. C_{oss} Charge @ Different Load Current.

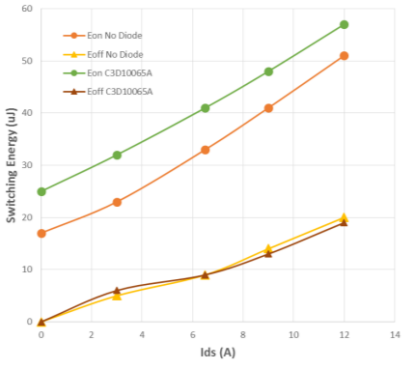


Fig. 14. Switching-loss Comparison w/n Anti-Parallel Diodes.

Secondly, even with ZVS turn-on, the TO-247/220 packaged diodes are much bulkier than HEMTs, which will complicate the heat sink design and obstruct the reduction of the loop inductance.

B. Hard-switched DC/DC Converter

To apply 650V GaN HEMTs to an 800V/400V DC-DC converter, a multi-level topology is an excellent candidate, as shown in Fig.15a. When S_1 and S_4 are turned on, the power is flowing from V_{in} to V_o. When S_1 and S_4 are off, the inductor current will freewheel through S_2 and S_3. Essentially this circuit acts as a hard-switched bidirectional buck/boost converter. Two 30A switches are paralleled.

In addition, a conventional buck converter using 1200V SiC MOSFETs is the backup candidate, as shown in Fig.15b. Assume all converters are running at 500kHz. The system loss breakdown of two different systems is shown as Fig.15c, indicating that the 650V GaN HEMT has great advantages on both the conduction and switching performance.

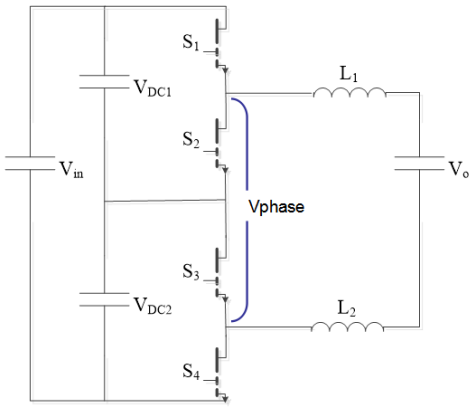


Fig. 15a. The Three-level Topology with 650V GaN HEMTs.

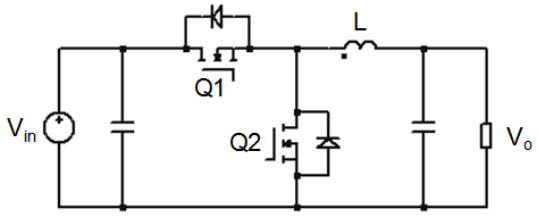


Fig. 15b. The Conventional Buck Converter with 1200V SiC MOSFETs.

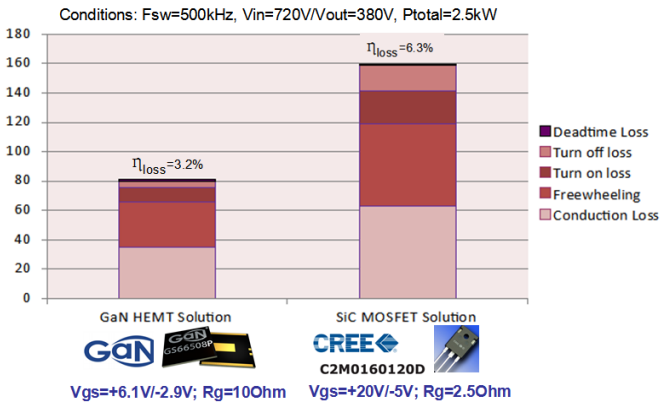


Fig. 15c. System Loss Breakdown Comparison between Two Solutions.

Such comparison of these two hard-switching converters is not aiming to compare these two types of WBG devices, given 1200V devices usually have much worse conducting and switching performance than low-voltage switches. This case validated that 1) GaN HEMTs could be used in hard switching, 2) external diode will increase the switching loss. Shown in Fig.16c, the increment of the switching-on loss is due to the reverse recovery current of Q_2 being added to the Q_1 turn-on current.

V. Conclusion

In this paper, the switching process of GaN HEMTs is thoroughly modelled and discussed to understand the effects of parasitics. Design rules for gate driver circuits and layout that affect the parallel operation are detailed. We put our focus particularly on the quasi-common-source inductance and flux canceling technique. The gate-drive circuit for GaN is also recommended.

The main contribution of this work includes 1) a half-bridge power stage was constructed using four GaN HEMTs in parallel, rated at 650V/240A, and 2) both soft switching and hard switching of the GaN HEMT are tested in the actual system. All of the above can only be realized after the thorough understanding of GaN HEMT dynamic processes, e.g., switching on/off processes, dead-band effect, extract of parasitics and optimization of the gate-drive design.

References

[1] X Huang, Q Li, Z Liu and F.C. Lee, "Analytical loss model of high voltage GaN HEMT in cascode configuration", *IEEE Transactions on Power Electronics*, vol. 29, no.5, pp. 2208–2219, 2014.

[2] A. Lidow and J. Strydom, "eGaN FET Drivers and Layout Considerations", pp.1–7, 2012, online.

[3] Z. Wang and J. Honea, " Investigation of Driver Circuits for GaN HEMTs in Leaded Packages", *IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pp. 81–87, 2014.

[4] Z. Liu, X Huang, F.C.Lee and Q. Li, "Package parasitic inductance extraction and simulation model development for the high-voltage cascode GaN HEMT", *IEEE Transactions on Power Electronics*, vol.29, no.4, pp.1977–1985, 2014.

[5] J. Lu and H.Bai, "Design Consideration of Gate Driver Circuits and PCB Parasitic Parameters of Paralleled E-Mode GaN HEMTs in Zero-Voltage-Switching Applications", APEC, pp.529 – 535, 2016.

[6] J. Lu, H. Bai, S. Averitt, D. Chen and J. Styles, "An E-mode GaN HEMTs based three-level bidirectional DC/DC converter used in Robert Bosch DC-grid system", 3rd IEEE Workshop on Wide Bandgap Power Devices and Applications, pp.334–340, 2015.

[7] Z. Wang, Y. Wu, J. Honea and L. Zhou, "Paralleling GaN HEMTs for Diode-free Bridge Power Converters", APEC, pp.752–758, 2015.

[8] F.Luo, Z.Chen, L.Xue, P.Mattavelli, D.Boroyevich and B.Hughes, "Design Considerations for GaN HEMT Multichip Half- bridge Module for High-Frequency Power Converters", APEC, pp.537-544, 2014.

[9] X. Zhang, N. Haryani, Z. Shen, R. Burgos and D. Boroyevich, "Ultra-Low Inductance Phase Leg Design for GaN-Based Three-Phase Motor Drive Systems", Workshop on Wide Bandgap Power Device and Applications, pp. 119-124, 2015.

[10] W. Kangping, M. Huan, L. Hongchang, G. Yixuan, Y. Xu, Z. Xiangjun and Y. Xiaoling, "An Optimized Layout with Low Parasitic Inductances for GaN HEMTs Based DC-DC Converter", APEC, pp. 948–951, 2015.

[11] Yuancheng Ren, Ming Xu, Jinghai Zhou, and Fred C. Lee, "Analytical Loss Model of Power MOSFET", *IEEE transactions on power electronics*, vol. 21, no. 2, march 2006.

[12] J. Lu, Q. Tian and H. Bai, “An Indirect Matrix Converter based 97% -efficiency On-board Level 2 Battery Charger Using E-mode GaN HEMTs”, 3rd IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA), pp. 351–358, 2015.

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