APPLICATION NOTE – GN006

# SPICE model for GaN HEMT- usage guidelines and example

As a development aid to ensure first pass design success, GaN Systems® provides PSpice and LTspice models for simulation. Because typical switching frequencies achievable with GaN Systems transistors are comparable with the response times associated with thermal phenomena, a complete electro-thermal model has been developed. This document describes the current release of the model, based on the measured characteristics of the GaN HEMTs. This document will be updated periodically as new devices are characterized and as new products are released.

The model has been developed for use with PSpice and LTspice. This document first describes the model, then provides instructions on how to import the model into PSpice and LTspice, and finally compares some test and simulation results.

## The model description

When properly loaded, following the instructions below, the transistor symbol will appear as in Figure 1.

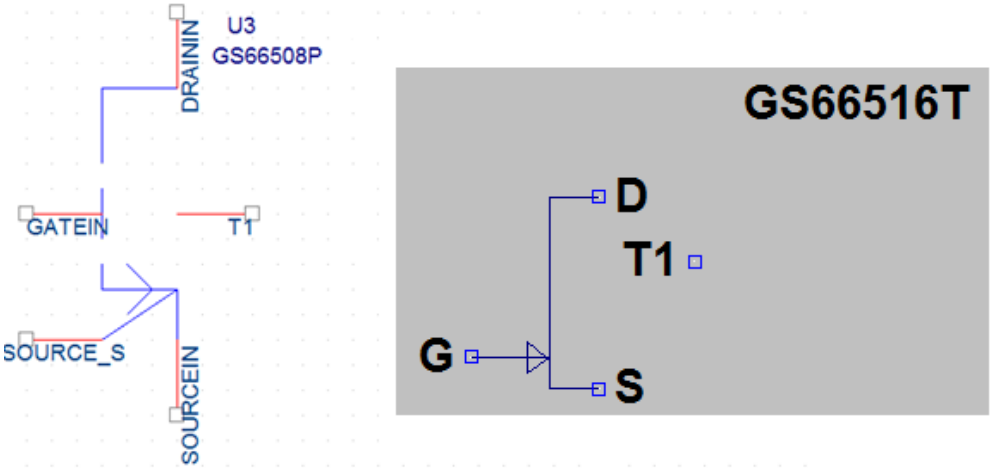
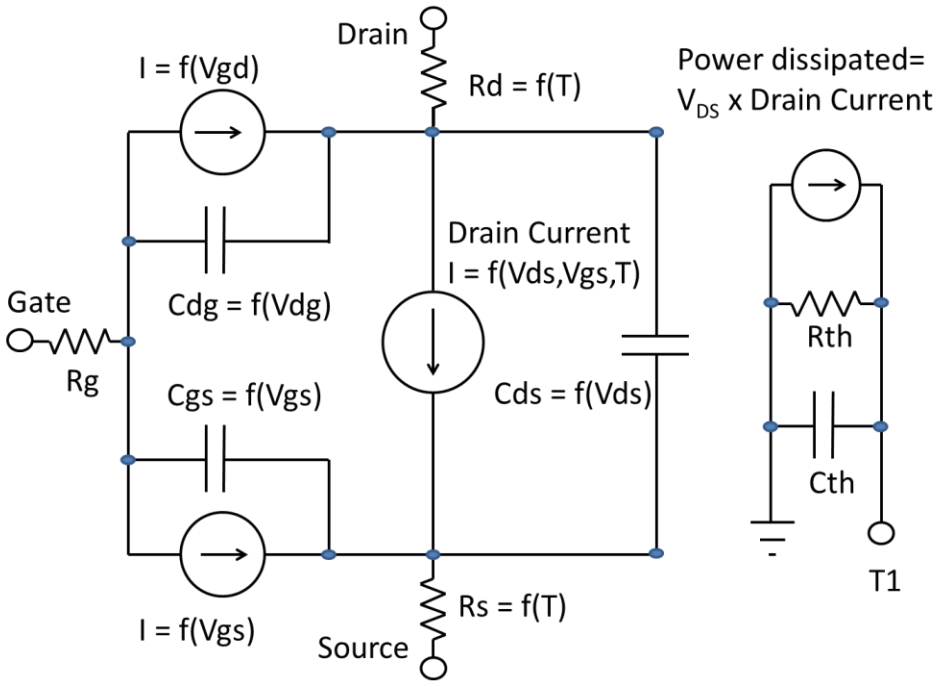



Figure 1: Transistor symbols – screen shots – single packaged transistors in PSpice and LTspice

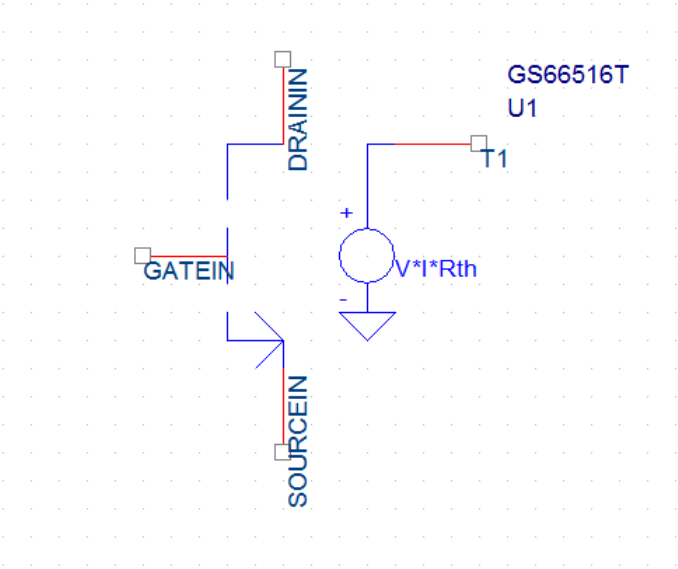
The thermal modeling is implemented with a separate thermal network, which allow for self-heating simulations to take place. A package level model is provided and the thermal impedance of the package is included in the model. **The T1 terminal should not be confused with the substrate connection.** The T1 terminal can be connected to ground (node zero) in order to disable self- heating altogether. If not connected to ground, the voltage at T1 will reflect the change in temperature relative to the reference temperature. The default temperature is 25˚C, but it can be changed in PSpice, using a ".step" statement (for example, the command ".step Temp 25 125 100" will run simulations at 25˚C and 125˚C). The model has been calibrated to include the temperature dependence of the saturation current and drain-to-source resistance.

Figure 2 shows a functional block diagram of the sub-circuit used. It consists of a voltage-controlled current source with a $V_{gs}$ and a $V_{ds}$ dependence. Series resistors are included as well as voltage dependent parasitic capacitors. The schematic also includes diodes used to model gate leakage current. A thermal network is used to determine the rise in temperature generated by self-heating. A thermal resistance (J. Joh et al., IEEE Trans. on Electron Devices, Vol. 56 No 12, Dec 2009) was derived for GaN Systems chips, based on thermal simulations performed using the Electroflo software package.




a)

Figure 2: Equivalent sub-circuit of HEMT model (a) and explicit symbol (b)




b)

The explicit symbol shown in figure 2b is not used in circuit simulation, but is presented here to clarify the separation of the electrical and thermal networks.

## Importing the part model into PSpice

The model contains two files, .lib and .olb. The .lib file contains **the model library**, and the .olb file contains **the part symbol**. The model is imported into PSpice in two major steps.
In STEP 1 the two files need to be imported into the PSpice Cadence tool.
In STEP 2 **the model library** needs to be added to the schematic, in which the part model is used, and to the simulation profile.
The following procedure describes the two steps in more details.

Step 1

1. Right click on the GaN_GS665XXX_Release1p27.lib file
2. Save the file in: C:\Cadence\SPB_16.6\tools\pspice\library
3. (If the Cadence tool is in the "Program Files" directory then the file needs to be saved in:
   C:\ Program Files\Cadence\SPB_16.6\tools\pspice\library)
4. Right click on the GaN_GS665XXX_Release1p27.OLB file
5. Save the file in: C:\Cadence\SPB_16.6\tools\capture\library\pspice

6. (If the Cadence tool is in the "Program Files" directory then the file needs to be saved in:
   C:\ Program Files\Cadence\SPB_16.6\tools\capture\library\pspice)

Step 2

1. Open the schematic in which the part model is to be used.
2. Click on Place -> Part.
3. Click on Add Library (Alt-A).
4. Browse to C:\Cadence\SPB_16.6\tools\capture\library\pspice
5. Find GaN_GS665XXX_Release1p27 and click on it.
6. Click on Open.
7. Click on GS665XXX to select the part.
8. Click on Enter – the part should appear in the schematic.
   (Steps 3, 7 and 8 are shown on Fig. **3**)
9. On the schematic page click on Edit Simulation Profile.
10. Click on Configuration Files.
11. Click on Library.
12. Click on Browse.
13. Browse to:
    C:\Cadence\SPB_16.6\tools\pspice\library\
    GaN_GS665XXX_Release1p27 Click on Add as Global.
14. Click on Apply.
15. Click on OK.
16. The part model should be ready for simulation.

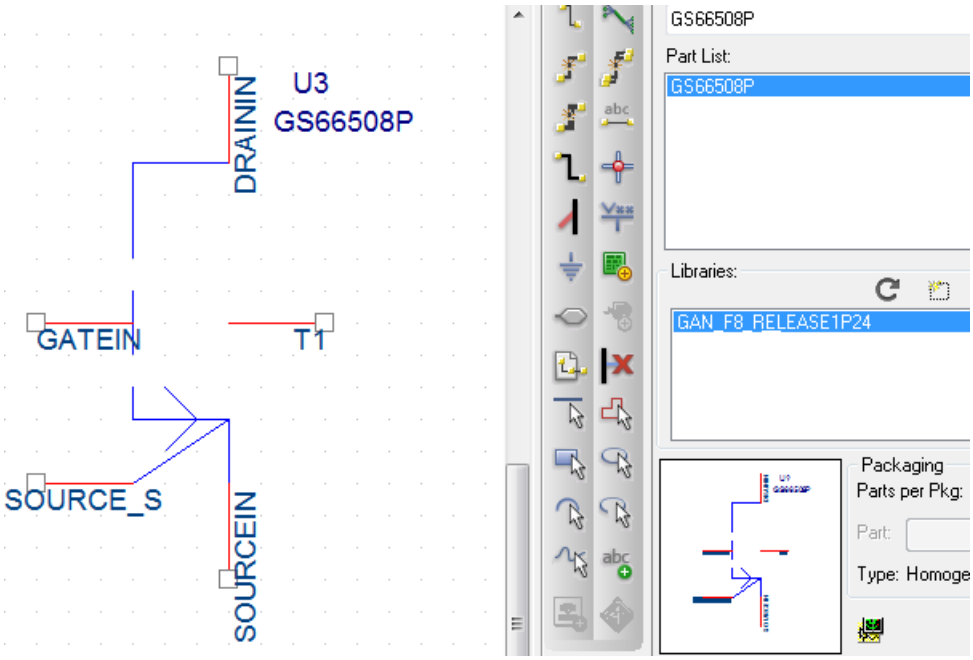


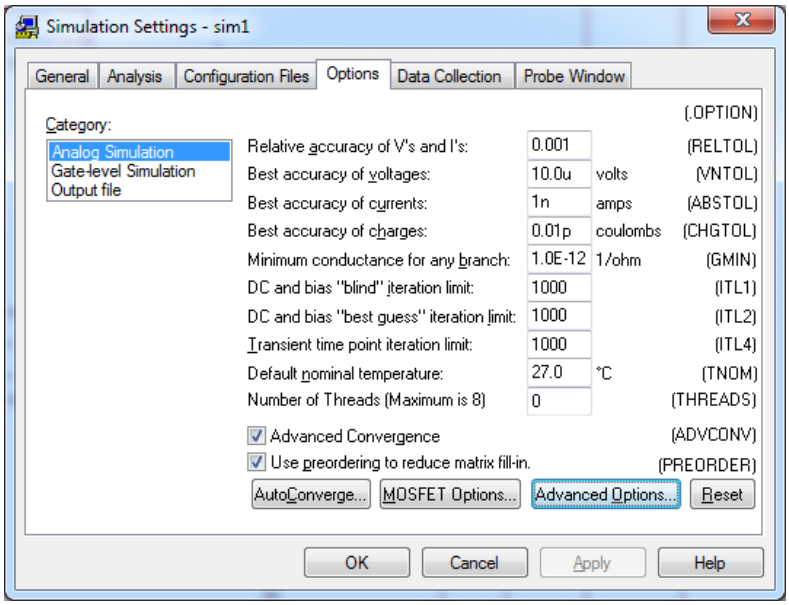

Figure 3: Adding the part into a schematic.

## Recommended PSpice settings

For the model to better converge it is recommended to adjust the PSpice parameters VNTOL to 10uV and ABSTOL to 1.0nA. The following steps describe how to adjust the two parameters:

1. On the schematic page click on Edit Simulation Profile.
2. Click on Options.
3. Change VNTOL to 10uV, and ABSTOL to 1.0nA.

Depending on the specific application some other parameters may need to be changed as well.
"Auto Converge" should be enabled to improve convergence. The maximum time step can modified if needed.
Typical option settings can be seen below.




## Test and simulation results

Figure 4 shows the IV output characteristics measured (solid traces) and simulated (dashed traces). A pulse width of 50µs was used for this measurement, limiting the amount of self- heating. Nevertheless, a small amount of self-heating is still taking place, resulting in a negative slope in the high current/high voltage region. Simulation is done with self-heating disabled.

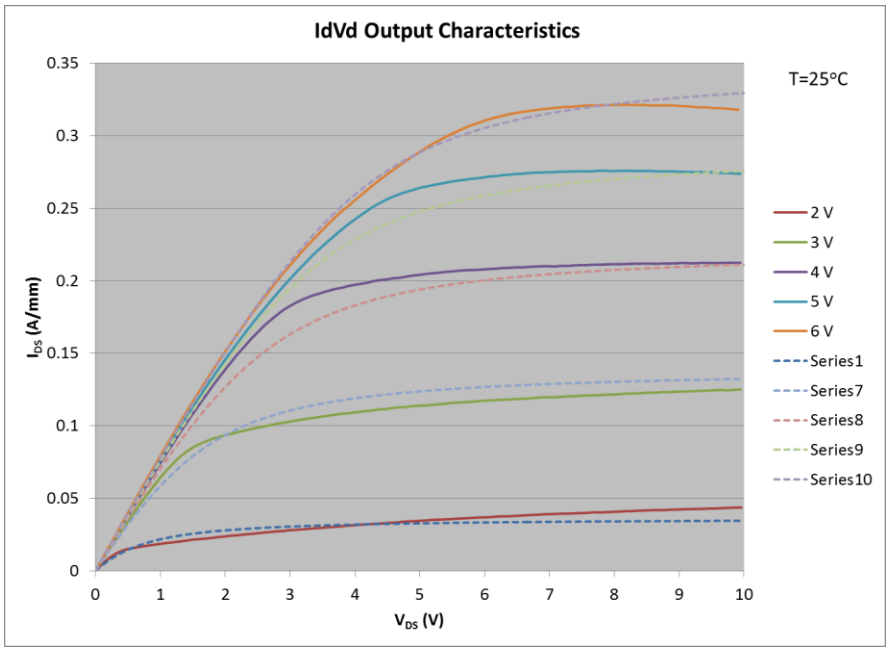



Figure 4: Example of measured (solid lines) and simulated (dashed lines) IV output characteristics. The negative output conductance at higher current/voltage is caused by self-heating.

The non-linear voltage-dependent capacitances between the different terminals of the device have been characterized using the capacitance meter attached to an Agilent B1505A curve tracer. The off-state capacitance values vary non linearly with applied voltage, and Figure 5 shows the values computed with the model, overlaid with actual measurements.

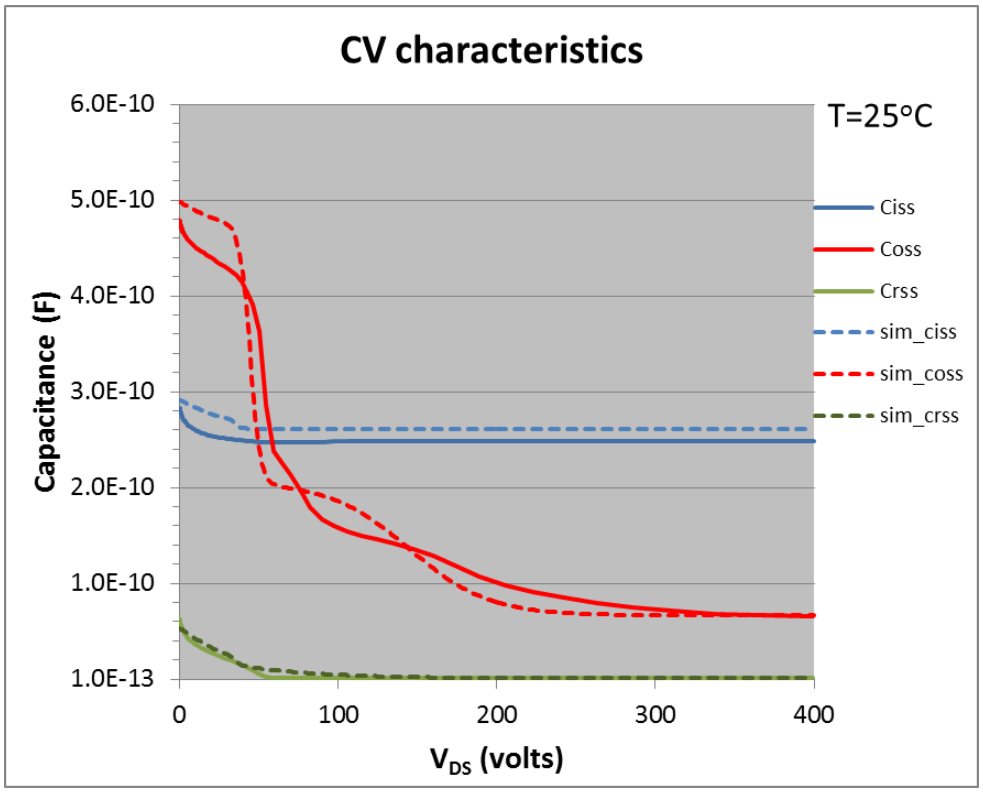



Figure 5: Off-state capacitances measured and simulated at $V_{GS}$=0 for increasing values of $V_{DS}$.

Figure 6 shows a typical half bridge implementation. In this case the self-heating circuit has been disabled on the high side device by connecting T1 to ground. **One should not connect T1 to the source** of the device in this case, since the thermal network is separate. The T1 terminal of the lower device is connected to a wire and used to monitor the temperature variation at the junction of that device.

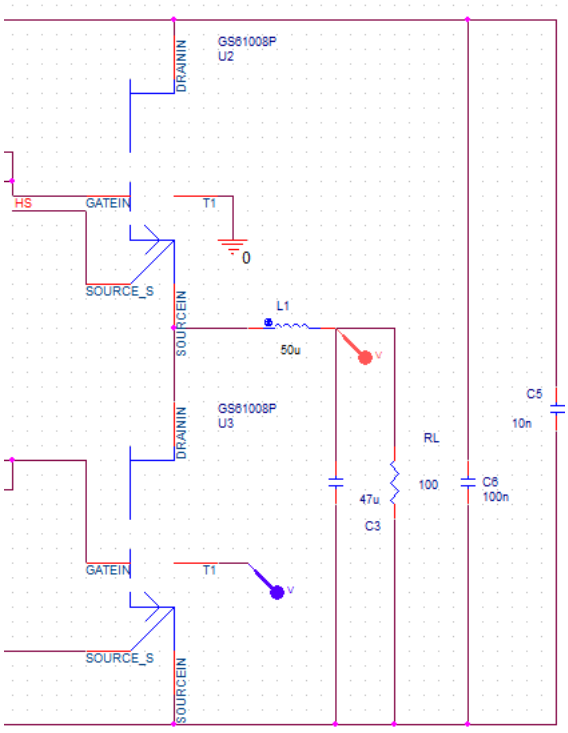



Figure 6 – Half bridge implementation

Figure 7 below shows a simple double pulse test switching circuit example. Significant amounts of inductance have been added to reflect parasitics. Figure 8 shows simulated waveforms for that circuit, including voltage overshoot and ringing caused by parasitic inductance.

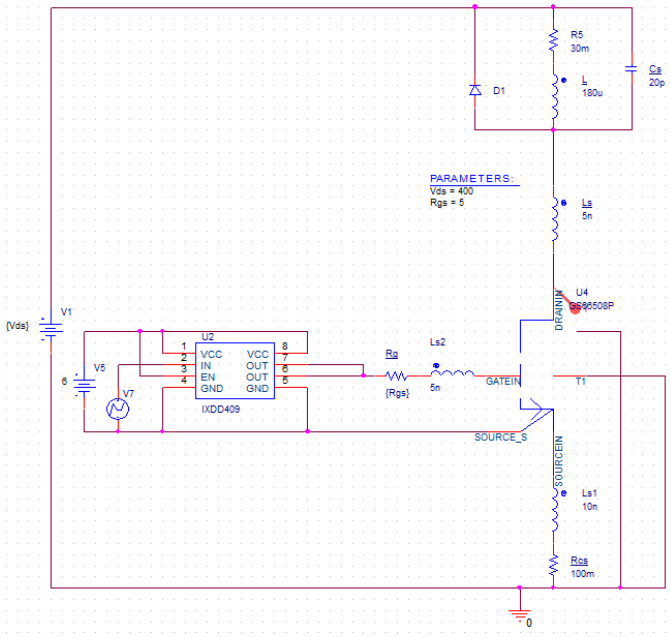



Figure 7: Simple double pulse switching circuit (GS66508P)

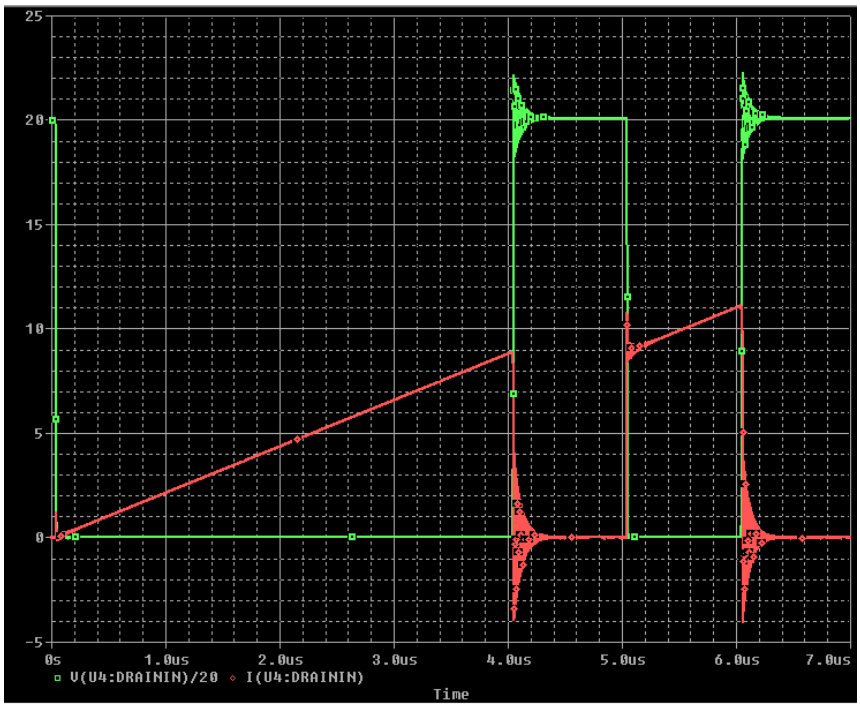
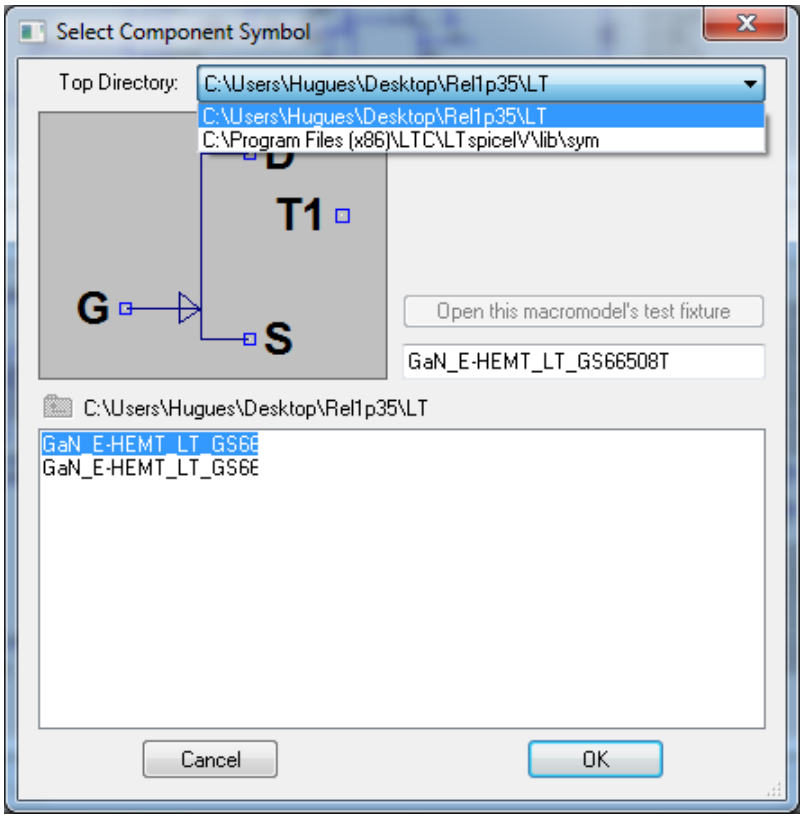



Figure 8: Simulated switching waveforms showing drain voltage (divided by 20) and current as a function of time.

## LTspice implementation

The model contains two files, .lib and .asy. The .lib file contains the model information, and the .asy file contains the symbol. Both files can be downloaded in a zip file and then extracted to the working directory, where the schematics is located. After creating a new schematics or opening an existing one in the working directory, go to the Edit menu and choose Components. The component window shown in Figure 9a) should open. Select the symbol and ok to add it to your schematics.

Several settings can be modified in LTspice. The following options in Figure 9b) have been used to consistently achieve convergence for half bridge power switch circuits.




a)

```
.tran 0 190u 0 0.1n
.option ITL1=500
.option ITL2=500
.option ITL4=500
.option RELTOL=0.01
.option ABSTOL=1E-09
.option CHGTOL=1E-12
.option VNTOL=1E-6
.option GMIN=1E-15
.option TRTOL=1
.option noopiter
.option gminsteps=0
.option topologycheck=0
.option temp=25
```

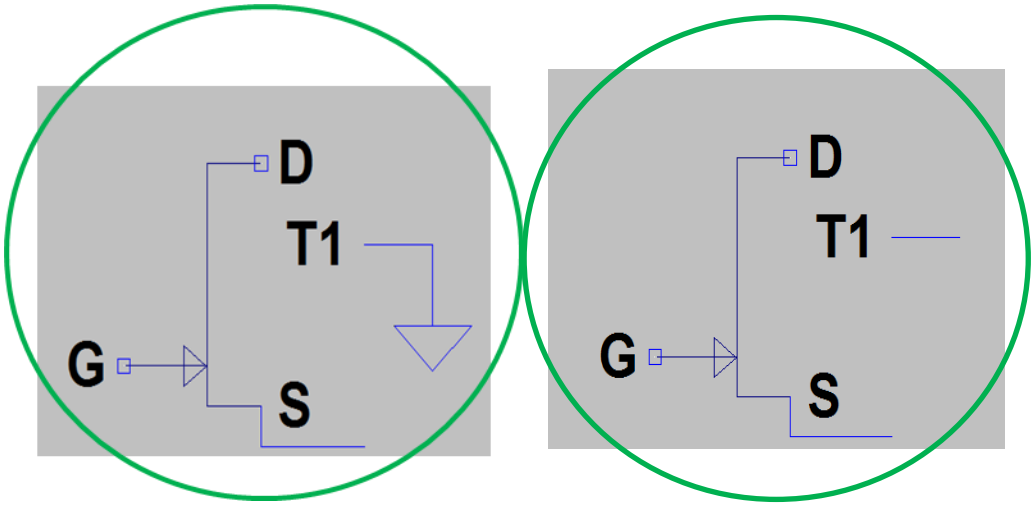
b)

Figure 9: a) How to add the GaN transistor to a schematics and b) Example of settings used to facilitate convergence in LTSpice

Similarly to the PSpice case, the use of the thermal node needs to be carefully considered. The thermal network should be treated separately from the electrical network, even though this is not explicitly shown in the simplified symbol. Figure 10 shows how to either disable the self-heating feature in the electro-thermal model (a). This connection is used to simulate a fixed junction temperature, as in the data sheet charts and specifications, and the T1 node should be connected to a separate ground in order to model this.

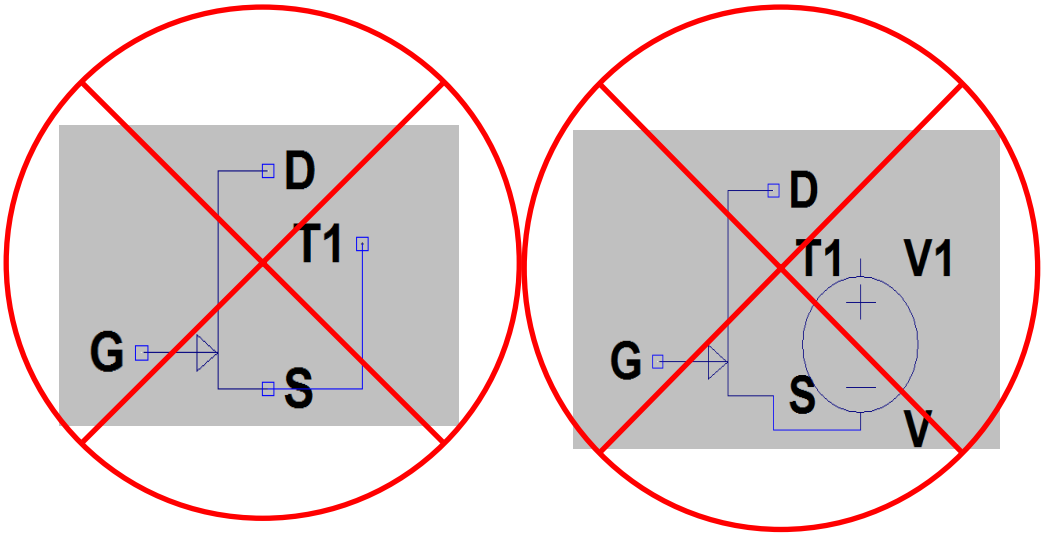
Figure 10 b) shows how to use the intended temperature change monitoring option. The node T1 is a sense terminal that monitors the rise in junction temperature, assuming a fixed case temperature. The change in junction temperature is then proportional to the power dissipated in the transistor.

Figure 11 shows various connections that should not be used as they would defeat the purpose of the model.




a) b)

Figure 10: Recommended use of the thermal pin to **disable self-heating** (a) or monitor the temperature delta (b) i.e. **V (T1) = dTemp**




a) b)

Figure 11: **Non recommended** use of the thermal pin

In summary, a GaN HEMT model has been implemented in PSpice and LTspice, showing good convergence for simulating switching circuits. This model will continue to be improved as more characterization history is collected.

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