IMS 2 Evaluation Platform

User’s Guide

GSP665HPMB-EVBIMS2
GSP66508HB-EVBIMS2
GSP66516HB-EVBIMS2

Visit www.gansystems.com for the latest version of this user’s guide.
DANGER

DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW ALL COMPONENTS TO DISCHARGE COMpletely PRIOR HANDLING THE BOARD.

HIGH VOLTAGE CAN BE EXPOSED ON THE BOARD WHEN IT IS CONNECTED TO POWER SOURCE. EVEN BRIEF CONTACT DURING OPERATION MAY RESULT IN SEVERE INJURY OR DEATH.

Please sure that appropriate safety procedures are followed. This evaluation kit is designed for engineering evaluation in a controlled lab environment and should be handled by qualified personnel ONLY. Never leave the board operating unattended.

WARNING

Some components can be hot during and after operation. There are NO built-in electrical or thermal protection on this evaluation kit. The operating voltage, current and component temperature should be monitored closely during operation to prevent device damage.

CAUTION

This product contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.
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1 Overview

1.1 Introduction

A frequent challenge for power designers is to engineer a product that has excellent power density while simultaneously reducing the cost of the system.

This IMS evaluation platform demonstrates an inexpensive way to improve heat transfer, to increase power density and reduce system cost. An Insulated Metal Substrate PCB (IMS PCB) is used to cool GaN Systems’ bottom-side cooled power transistors. An IMS PCB is also known as Metal Core/Aluminum PCB.

Examples of applications that have successfully used this approach include:

- **Automotive:** 3.3kW-22kW on board charger, DC/DC, 3-Φ inverter, high power wireless charger
- **Industrial:** 3-7kW Photovoltaic Inverter and Energy Storage System (ESS), Motor Drive / VFD
- **Server/Datacenter:** 3kW Server ACDC power supply.
- **Consumer:** Residential Energy Storage System (ESS)

This evaluation platform consists of two parts: the IMS 2 EVB board (mother board) and the IMS 2 half bridge power board, as show in Figure 1. The IMS 2 half bridge power board is available in 2 power levels: 3kW and 6kW.

A suitable heatsink is included for lower power applications. For higher power applications additional heatsinking may be required. To prevent device damage, ensure adequate heatsinking through design and by monitoring the component temperatures during operation.

To assemble a heatsink, apply thermal grease to the heatsink / IMS board interface before screwing the units together. Enough thermal grease should be applied so that a small amount extrudes on all four sizes as the screws are tightened. Wipe the assembly clean.

With these building blocks, the evaluation platform can be purchased in 4 different configurations: low power and high power, half bridge and full bridge. Table 1 lists the ordering options.
### Table 1 Ordering configuration and part numbers

<table>
<thead>
<tr>
<th>CONFIGURATION</th>
<th>IMS 2 HALF BRIDGE MODULE</th>
<th>IMS 2 EVB Mother Board</th>
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<tbody>
<tr>
<td>3 kW Half Bridge</td>
<td>QTY 1 - GSP66508HB-EVBIMS2</td>
<td>QTY 1: GSP665HPMB-EVBIMS2</td>
</tr>
<tr>
<td>6 kW Half Bridge</td>
<td>QTY 1 - GSP66516HB-EVBIMS2</td>
<td></td>
</tr>
<tr>
<td>3 kW Full Bridge</td>
<td>QTY 2 - GSP66508HB-EVBIMS2</td>
<td></td>
</tr>
<tr>
<td>6 kW Full Bridge</td>
<td>QTY 2 - GSP66516HB-EVBIMS2</td>
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### Table 2 Part numbers and Description

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<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>GaN E-HEMT</th>
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</thead>
<tbody>
<tr>
<td>GSP665HPMB-EVBIMS2</td>
<td>Optimized Dual HB Gate Driver Motherboard with isolated driver and PSU for use with GSP66516HB-EVBIMS2 or GSP66508HB-EVBIMS2 half bridge boards</td>
<td>N/A</td>
</tr>
<tr>
<td>GSP66508HB-EVBIMS2</td>
<td>Optimized IMS 2 Half Bridge based on GS66508B GaNPX® bottom-cooled E-HEMTs</td>
<td>GS66508B</td>
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<tr>
<td>GSP66516HB-EVBIMS2</td>
<td>Optimized IMS 2 Half Bridge based on GS66516B GaNPX® bottom-cooled E-HEMTs</td>
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### 1.2 IMS 2 Evaluation Platform Overview

#### 1.2.1 Technical Description

Using this platform, power designers can evaluate the performance of GaN Systems’ E-HEMTs (Enhancement mode High Electron Mobility Transistors) in high power, high efficiency applications. The IMS 2 half bridge power board is populated with GaN Systems’ GS66516B (bottom-side cooled E-HEMT, rated at 650 V / 25 mΩ) or GS66508B (bottom-side cooled E-HEMT, rated at 650 V / 50 mΩ). The embedded GaNPX® SMD package has the following features:

- Large power source/thermal pad for improved thermal dissipation.
- Bottom-side cooled packaging for conventional PCB or advanced IMS/Cu inlay thermal design.
- Ultra-low inductance for high frequency switching.

![Figure 2 - GS66516B and GS66508B GaNPX® packaged E-HEMTs](image)
The IMS 2 half bridge power board is designed for users to gain hands-on experience in the following ways:

- Evaluate the GaN E-HEMT performance in any half bridge based topology, over a range of operating conditions. This can be done using either the accompanying power motherboard (P/N: GSP665HPMB-EVBIMS2) or with the users’ own board for in-system prototyping.
- Use as a thermal and electrical design reference of the GS66516B or GS66508B GaNPX® package in demanding high-power applications.

1.2.2 IMS Board thermal design

An IMS board assembly uses metal as the PCB core, to which a dielectric layer and copper foil layers are bonded. The metal PCB core is often aluminum. The copper foil layers can be single or double-sided. An IMS board offers superior thermal conductivity to standard FR4 PCB. It’s commonly used in high power, high current applications where most of heat is concentrated in a small footprint SMT device.

As high-speed Gallium Nitride power devices are adopted widely, the industry is trending away from through-hole packaging (TH), towards surface mount packaging (SMT). Traditional TH devices, such as the TO-220, are no longer the appropriate choice because their high parasitic inductance and capacitance negate the performance benefits offered by GaN E-HEMTs. SMT packaging, such as PQFN, D2PAK and GaN Systems’ GaNPX®, by comparison, offer low inductance and low thermal impedance, enabling efficient designs at high power and high switching frequency.

Thermal management of SMT power transistors must be approached differently than TH devices. TO packages are cooled by attaching them to a heatsink, with an intermediary Thermal Interface material (TIM) sheet for electrical high voltage insulation. The traditional cooling method for SMT power devices is to use thermal vias tied to multiple copper layers in a PCB. The IMS board presents designers with another option which is especially useful for high power applications. The IMS board has a much lower junction to heatsink thermal resistance (R_{thJ-HS}) than FR4 PCBs, for efficient heat transfer out of the transistor. As well, assembly on an IMS board has lower assembly cost and risk than the TH alternative. The manual assembly process of a TO package onto a heatsink is costly and prone to human error.

Table 3 compares 3 different design approaches for cooling discrete SMT power devices. While the cost is lower for a FR4 PCB cooling with thermal vias, the IMS board offers the best performance for thermal management.
management Figure 4 provides a quantitative comparison of the thermal resistance for the 3 design options. The IMS board clearly comes out ahead.

Table 3 Performance comparison of 3 thermal design options for SMT power devices

<table>
<thead>
<tr>
<th>Design</th>
<th>FR4 PCB Cooling with Vias</th>
<th>FR4 PCB with Cu inlay</th>
<th>IMS PCB</th>
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<tbody>
<tr>
<td>Thermal resistance</td>
<td>Good</td>
<td>Better</td>
<td>Best</td>
</tr>
<tr>
<td>Electrical Insulation</td>
<td>No, additional TIM needed</td>
<td>No, additional TIM needed</td>
<td>Yes</td>
</tr>
<tr>
<td>Cost</td>
<td>Lowest</td>
<td>High</td>
<td>Low</td>
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<tr>
<td>Advantages</td>
<td>• Standard process</td>
<td>• Layout flexibility</td>
<td>• Lowest thermal resistance</td>
</tr>
<tr>
<td></td>
<td>• Lowest cost</td>
<td>• Improved thermal</td>
<td>• Electrically isolated</td>
</tr>
<tr>
<td></td>
<td>• Layout flexibility</td>
<td>compared to thermal</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>vias</td>
<td></td>
</tr>
<tr>
<td>Design challenges</td>
<td>• High PCB thermal</td>
<td>• Cu-inlay surface</td>
<td>• Layout limited to 1</td>
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<tr>
<td></td>
<td>resistance</td>
<td>coplanarity</td>
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<td></td>
<td></td>
<td>• High TIM thermal</td>
<td>• Parasitic inductance</td>
</tr>
<tr>
<td></td>
<td></td>
<td>resistance</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Coupling capacitances</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>to the metal substrate</td>
</tr>
</tbody>
</table>

Figure 4 Comparison of Junction to Heatsink thermal resistance ($R_{\text{thJ-HS}}$) (Estimated based on GS66516B)
The following additional measures are taken to optimize the design further.

- The IMS 2 evaluation platform is implemented as a two-board assembly. The gate drive circuitry is assembled on the GSP665HPMB-EVBIMS2, a multi-layer FR4 PCB mother board. This includes the gate driver ICs, an isolated push-pull power supply to power the driver IC, and DC decoupling capacitors. The GaN E-HEMTs are mounted to the IMS half bridge board (GSP66508HB-EVBIMS2 and GSP66516B-EVBIMS2). This approach addresses the shortcomings of implementing the design on a single layer IMS board.

- While a large copper area is preferred to maximize heat spreading and handle high current, the area of copper at the switching node (high dv/dt) needs to be minimized to reduce the parasitic coupling capacitance to the metal substrate. An IMS board with thicker dielectric layer (100um) is chosen on this design to further reduce this effect.

1.3 IMS 2 Half Bridge Board Design

The IMS 2 half bridge power board is populated with the following components:

- **Q1 and Q2:** GS66516B or GS66508B E-HEMTs in a half bridge configuration.
  - 6kW GSP66516HB-EVBIMS2: Q1/Q2 GS66516B.
  - 3kW GSP66508HB-EVBIMS2: Q1/Q2 GS66508B.

- **J1, J2, J3:**
  - Connector Header Surface Mount 12 position 0.050” (1.27mm) (Samtec Inc., P/N: FTS-106-02-F-DV).
  - These terminals are designed to carry the main current and gate signals.
1.4 IMS 2 EVB Mother Board

GaN Systems offers a high-power IMS 2 evaluation board that can be purchased separately. The ordering part number is GSP665HPMB-EVBIMS2. It can be used as a platform for evaluating the IMS board in any half or full bridge topology.

![Circuit block diagram of IMS 2 EVB board](image1)

![GSP665HPMB-EVBIMS2](image2)
1.4.1 Gate Driver Circuit

A low cost isolated gate driver circuit is used in the IMS 2 EVB board for each GaN device, which is shown in Figure 8:

- U1 is the isolated gate driver (Silicon Labs P/N: Si8271)
- U2, T1, D1, C6, C7, C8 and U3 are the isolated push-pull power supply for the gate driver; after the LDO chip U3, the output is divided to +6/-3V to power the gate driver.
- R1 and R2 are gate turn-on and off resistors.

1.4.2 5V input

The gate driver circuit on the IMS 2 EVB mother board is powered from a 5V DC source, through connector J2.

1.4.3 Temperature monitoring holes

4 holes are located on the center of 4 GaN E-HEMTs to assist with the temperature monitoring during operation. A thermal camera can be used to monitor the case temperature through these holes. The temperature measured at the center of GaNPX® package will be close to the TJ.

NOTE: Thermal performance of the transistors is dependent on a number of factors including circuit configuration, ambient temperature, airflow, and heatsinking. The user is responsible for monitoring the temperature of the devices to ensure operation remains within specification.
1.4.4  External PWM Signals Input

The PWM signals of all four GaN devices come from the external PWM connector J1, as shown in Figure 9. The deadtime of PWM signals are required and should be provided from the external source.

1.4.5  Installation of IMS 2 Half Bridge Power Board

To achieve the lowest power loop parasitics, it is suggested to solder the IMS 2 half bridge power board to the IMS 2 EVB motherboard.

1.4.6  DC link decoupling capacitors

As it is challenging to create low inductance power loop on single-layer IMS board, DC decoupling capacitors are placed on multi-layer IMS 2 EVB PCB. The power loop path is highlighted as below.
1.4.7 Operation modes

The Evaluation Platform can be configured into different topologies and operation modes as shown below.

<table>
<thead>
<tr>
<th>HALF BRIDGE</th>
<th>FULL BRIDGE</th>
<th>BOOST MODE</th>
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<td><strong>Double Pulse Test</strong></td>
<td><strong>Full Bridge LLC</strong></td>
<td><strong>Synchronous Boost DC/DC</strong></td>
</tr>
<tr>
<td><img src="image1" alt="Diagrams" /></td>
<td><img src="image2" alt="Diagrams" /></td>
<td><img src="image3" alt="Diagrams" /></td>
</tr>
<tr>
<td><strong>Synchronous Buck DC/DC</strong></td>
<td><strong>Phase Shift Full Bridge</strong></td>
<td><strong>Totem Pole PFC</strong></td>
</tr>
<tr>
<td><img src="image4" alt="Diagrams" /></td>
<td><img src="image5" alt="Diagrams" /></td>
<td><img src="image6" alt="Diagrams" /></td>
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<tr>
<td><strong>Half Bridge LLC</strong></td>
<td><strong>Full Bridge Inverter</strong></td>
<td><strong>Interleaved Totem Pole PFC</strong></td>
</tr>
<tr>
<td><img src="image7" alt="Diagrams" /></td>
<td><img src="image8" alt="Diagrams" /></td>
<td><img src="image9" alt="Diagrams" /></td>
</tr>
<tr>
<td><strong>Single Phase Half Bridge Inverter</strong></td>
<td><strong>DUAL ACTIVE BRIDGE</strong></td>
<td><strong>Dual Active Bridge (with 2 mother boards)</strong></td>
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<td><img src="image10" alt="Diagrams" /></td>
<td><img src="image11" alt="Diagrams" /></td>
<td><img src="image12" alt="Diagrams" /></td>
</tr>
</tbody>
</table>
2 Test Results

2.1 Double pulse test (GSP665HPMB-EVBIMS2 + GSP66508HB-EVBIMS2)

- Test condition: \(V_{DS} = 400\text{V}, I_D = 30\text{A}, V_{GS} = +6\text{V}/-3\text{V}, L = 37\mu\text{H}, \) No RC Snubber, \(T_J = 25^\circ\text{C}\)
- Measured peak \(V_{DS} = 550\text{V}\) and 95.5V/ns peak \(dV/dt\)
- Reliable hard switching with GSP66508B is achieved at full rated current

![Double pulse test setup](image)

**Figure 11 Double pulse test setup**

![Double pulse test waveforms](image)

**Figure 12 Double pulse test waveforms (400V/30A)**
2.2 Full power emulation test (GSP665HPMB-EVBIMS2 + GSP66508HB-EVBIMS2)

- Test condition: $V_{\text{IN}} = 400\text{V}$, $f_{\text{sw}} = 500\text{kHz}$, $P_{\text{o}} = 1\text{kW}$, $T_{\text{AMB}} = 25^\circ\text{C}$.
- Device case temperature 57$^\circ\text{C}$
Ch#3 (purple): Inductor current, 2A/div
Ch#4 (green): Switching node Voltage, 250V/div

Figure 15 Test waveforms (400Vin, 500kHz, Po=1.2kW)
3 Appendix

3.1 IMS 2 Half Bridge Power Board

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**IMS 2 half bridge power board schematics**
(for GSP66508HB-EVBIMS2)

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**IMS 2 half bridge power board schematics**
(for GSP66516HB-EVBIMS2)

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**IMS 2 half bridge power board assembly drawing**
(for GSP66508HB-EVBIMS2)

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**IMS 2 half bridge power board assembly drawing**
(for GSP66516HB-EVBIMS2)
## IMS 2 Half Bridge Power Board Bill of Materials (BOM)

### GSP66508HB-EVBIMS2

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<th>Description</th>
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<td>FTS-106-02-X-DV</td>
<td>CONN HEADER SMD 12POS 1.27MM</td>
<td>J1, J2, J3</td>
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<td>Samtec Inc.</td>
<td>FTS-106-02-F-DV</td>
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<tr>
<td>GS66508B</td>
<td>GAN TRANS E-MODE 650V 30A</td>
<td>Q1, Q2</td>
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### GSP66516HB-EVBIMS2

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<td>GAN TRANS E-MODE 650V 60A</td>
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3.2 IMS 2 EVB Mother board - GSP665HPMB-EVBIMS2

IMS 2 EVB mother board schematics – GSP665HPMB-EVBIMS2
IMS 2 EVB mother board assembly drawing (top layer) - GSP665HPMB-EVBIMS2
### IMS 2 EVB mother board Bill of Materials (BOM) – GSP665HPMB-EVBIMS2

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<th>Description</th>
<th>Quantity</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
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<td>KEMET</td>
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<td>C4, C12, C20, C28</td>
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<td>C5, C13, C21, C29</td>
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<td>MCC</td>
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<td>U1, U4, U7, U10</td>
<td>DGTL ISO 2.5KV GATE DRV 8SOIC</td>
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<td>U3, U6, U9, U12</td>
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