

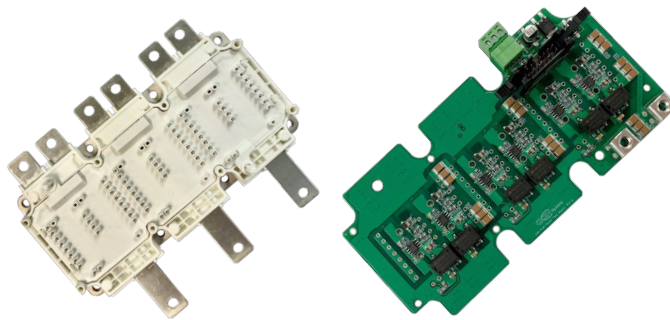
## GS-EVx-3PH-650V300A-SM1x

GS-EVM-3PH-650V300A-SM1

GS-EVB-3PH-650V300A-SM1A

### 650V 300A 3-Phase GaN Power Module with External Gate Driver Board

#### Technical Manual



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**WARNING:**

PCB surface can become hot. Contact may cause burns. Do not touch!



**CAUTION!**

This product contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.

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## Overview

The GS-EVM-3PH-650V300A-SM1 is 650V 300A 3-Phase GaN Power Module. This GS-EVM-3PH-650V300A-SM1 evaluation module is designed to meet high robustness, high power density, and low-cost requirements of the automotive and industrial markets. The GS-EVB-3PH-650V300A-SM1A is the external gate driver board for the 650V 300A 3-Phase GaN power module GS-EVM-3PH-650V300A-SM1. They are created in partnership with SilverMicro and intended for testing and evaluation purposes only.

## Features

➤ GS-EVM-3PH-650V300A-SM1

- Includes 12 GS-065-150-1-D (650V 150A E-mode Die)
- Industry standard form factor
- High thermal conductivity base plate
- External gate driver board
- Ultra-low switching losses & Zero  $Q_{RR}$
- Ultra-high dV/dt ruggedness
- Adjustable  $T_{RISE}$  /  $T_{FALL}$  & reverse conduction capability
- Press-Fit Pins for ease of assembly
- ZTA substrates for superior reliability
- Greater than 4 kV DC 1-second electrical Isolation

➤ GS-EVB-3PH-650V300A-SM1A

- Optimized & isolated 3-phase gate drive
- Single 5V input
- Ultra-high dV/dt ruggedness 200V/ns

## Applications

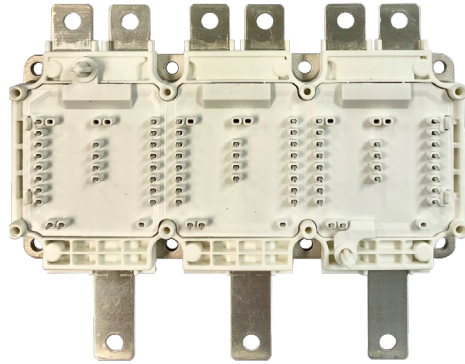
- High efficiency 75kW traction inverter drives
- Motor drives
- High efficiency high power density systems

**Contents**

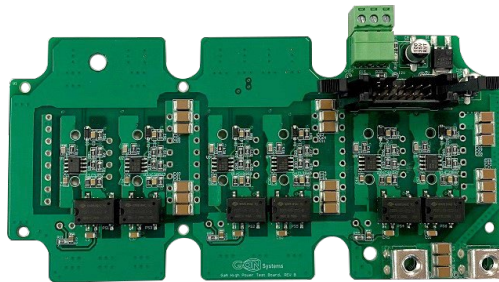
The GS-EVx-3PH-650V300A-SM1x includes the following hardware.

**Table 1 GS-EVx-3PH-650V300A-SM1x Evaluation Kit Contents**

Quantity	Description
1	GS-EVM-3PH-650V300A-SM1 650V 300A 3-Phase GaN Power Module
1	GS-EVB-3PH-650V300A-SM1A 650V 300A 3-Phase Driver Board



**Figure 1 650V 300A GaN 3 phase Power Module**



**Figure 2 External Gate Driver Board**

## Technical Specifications

### Block Diagram of Power Module

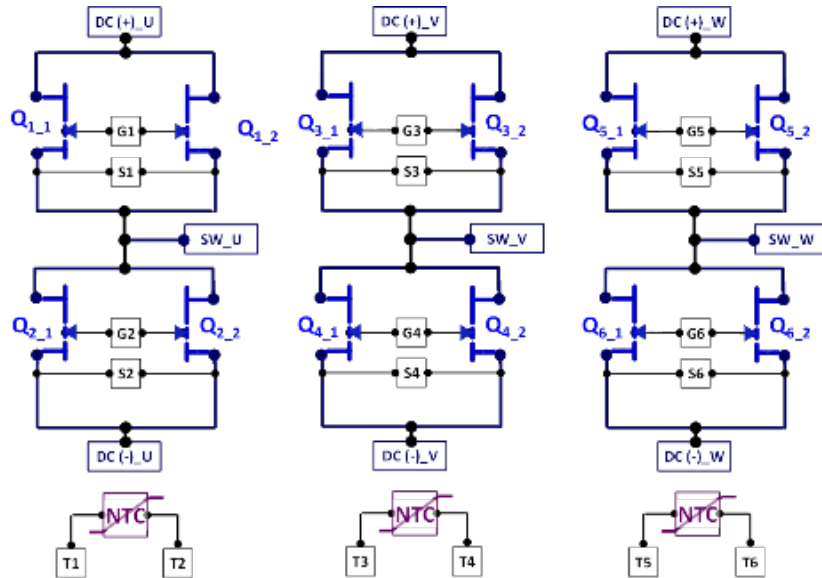


Figure 3 650V 300A GaN 3 phase Power Module Block Diagram

### Driver Board Pin Description

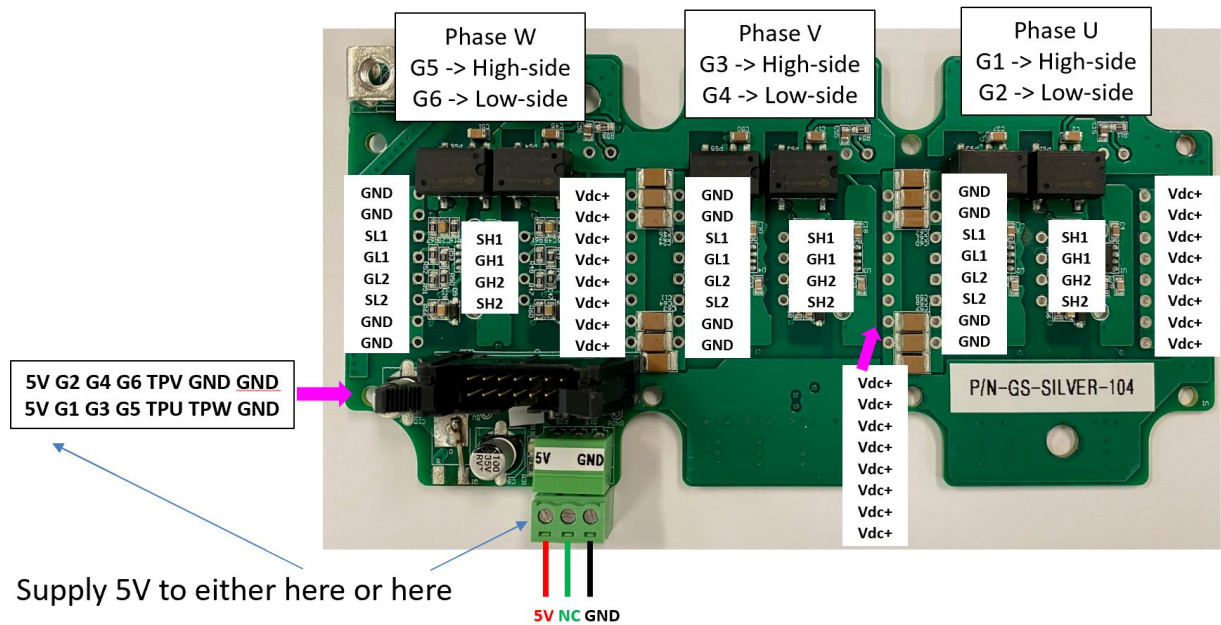
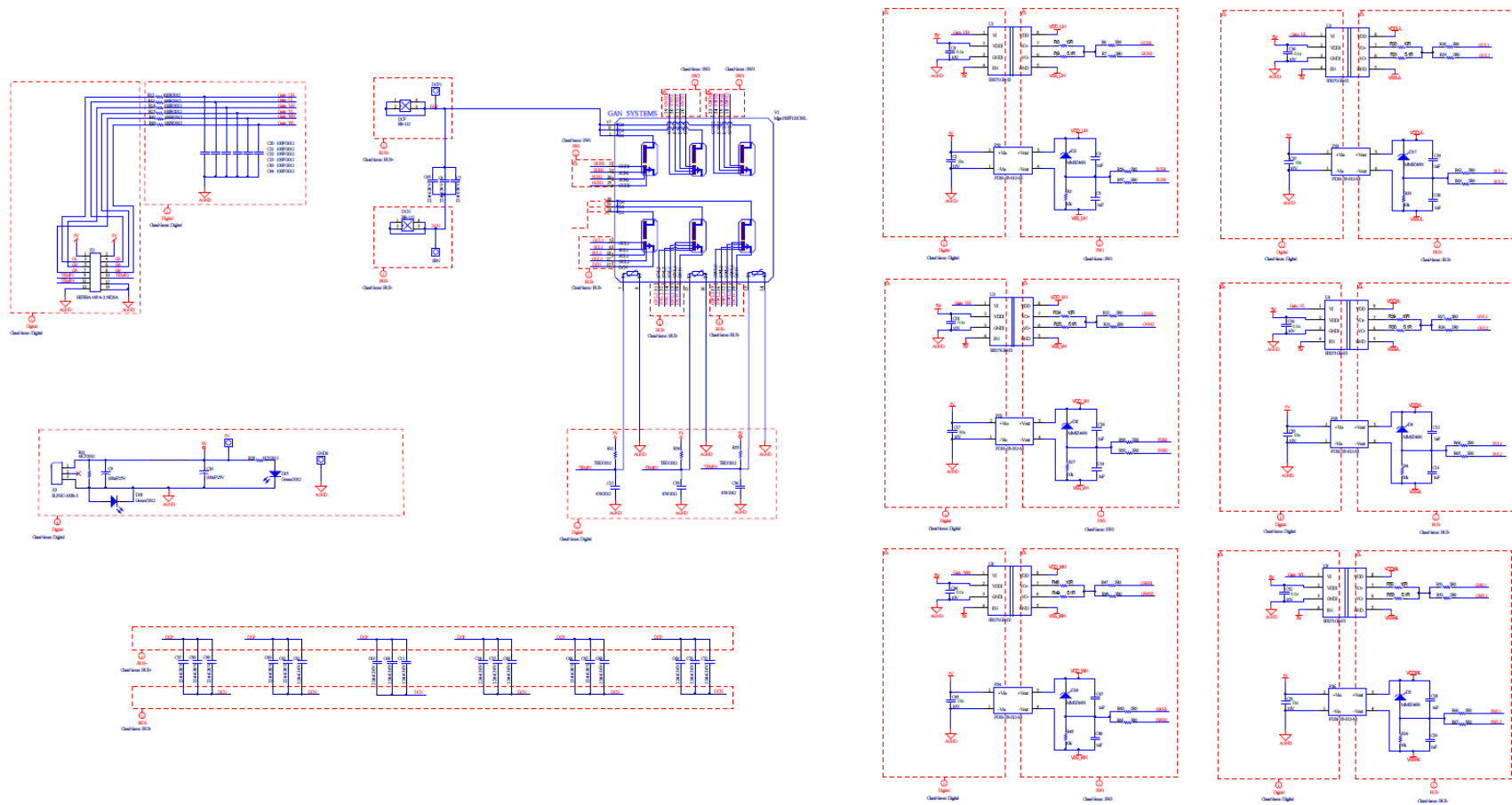


Figure 4 Driver Board Pin Description

**Driver Board Schematics**



**Figure 5 Driver Board Schematics**

### Electrical Characteristics

Test Conditions, unless otherwise noted:  $T_{JUNC} = 25^{\circ}C$ ,  $V_{GS} = 6.0V$

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	$V_{(BL)DSS}$	650	-	-	V	$V_{GS} = 0V$ , $I_{DS} < 560 \mu A$
Module ON Resistance $T_{JUNC} = 25^{\circ}C$	$R_{ON}$	-	6	7.5	$m\Omega$	$V_{GS} = 6.0V$ , $I_{DS} = 100A$ $T_{JUNC} = 25^{\circ}C$
Module ON Resistance $T_{JUNC} = 150^{\circ}C$ (Note 4)	$R_{ON}$	-	14	-	$m\Omega$	$V_{GS} = 6.0V$ , $I_{DS} = 100A$ $T_{JUNC} = 150^{\circ}C$
Drain-to-Source Leakage $T_{JUNC} = 25^{\circ}C$	$I_{DSS}$	-	22	550	$\mu A$	$V_{GS} = 0V$ , $V_{DS} = 650V$ $T_{JUNC} = 25^{\circ}C$
Drain-to-Source Leakage $T_{JUNC} = 150^{\circ}C$ (Note 4)	$I_{DSS}$	-	4400	-	$\mu A$	$V_{GS} = 0V$ , $V_{DS} = 650V$ $T_{JUNC} = 150^{\circ}C$
Gate-to-Source Threshold	$V_{GS(TH)}$	1.1	1.7	2.6	V	$V_{GS} = V_{DS}$ , $I_{DS} = 40mA$
Gate-to-Source Leakage	$I_{GSS}$	-	1822	-	$\mu A$	$V_{GS} = 6.0V$ , $V_{DS} = 0V$
Input Capacitance	$C_{ISS}$	-	2962	-	pF	$V_{GS} = 0V$ $V_{DS} = 400V$ $f = 100kHz$
Output Capacitance	$C_{OSS}$	-	740	-	pF	
Reverse Transfer Capacitance	$C_{RSS}$	-	22	-	pF	
Total Gate Charge	$Q_G$	-	66	-	nC	$V_{GS} = -3V$ to $6V$ $V_{DS} = 400V$
Gate-to-Source Charge	$Q_{GS}$	-	26	-	nC	
Gate-to-Drain Charge	$Q_{GD}$	-	20	-	nC	
Output Charge	$Q_{OSS}$	-	650	-	nC	$V_{GS} = 0V$ , $V_{DS} = 400V$
Reverse Recovery Charge	$Q_{RR}$		Zero		nC	N/A

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Turn-On Delay Time	$t_{D(ON)}$	-	<i>tbd</i>	-	ns	$V_{GS} = -3V$ to $6V$ , $V_{DS} = 400V$ , $I_{DS} = 160A$ , $R_{G(ON)} = 5\Omega$ , $T_{JUNC} = 25\text{ }^{\circ}C$ (Note 5)
Rise Time	$t_{RISE}$	-	<i>tbd</i>	-	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	-	<i>tbd</i>	-	ns	
Fall Time	$t_{FALL}$	-	<i>tbd</i>	-	ns	
Turn-On Switching Energy	$E_{ON}$	-	715	-	$\mu J$	$V_{GS} = -3V$ to $6V$ , $V_{DS} = 400V$ , $I_{DS} = 150A$ , $R_{G(ON)} = 10\Omega$ , $R_{G(OFF)} = 1\Omega$ , $L = 40\mu H$ (Note6)
Turn-Off Switching Energy	$E_{OFF}$	-	115	-	$\mu J$	

(Note 4) No manufacturing test (specified by design)

(Notes 5, 6) See diagrams in applications section for switching tests methodology

### Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction Temperature Range	$T_{JUNC}$	-	-	-55 to +150	$^{\circ}C$
Thermal Resistance, Junction-to-Cold Plate	$R_{\theta\_JUNCTION-COLD\ PLATE}$	-	0.20	-	$^{\circ}C/W$
Storage Temperature Range	$T_{STOR}$	-	-	-40 to +125	$^{\circ}C$

### NTC Characteristics

Parameter	Conditions / Equation	Typical Value	Units
$R_{25}$	$T_C = 25\text{ }^{\circ}C$	5	$k\Omega$
$\Delta R/R$	$T_C = 100\text{ }^{\circ}C$ , $R_{100} = 481\Omega$	$\pm 5$	%
$P_{25}$	$T_C = 25\text{ }^{\circ}C$	50	mW
$B_{25/50}$	$R_2 = R_{25} \exp[B_{25/50}(1/T_2 - 1/(298.15K))]$	3380	KW
$B_{25/80}$	$R_2 = R_{25} \exp[B_{25/80}(1/T_2 - 1/(298.15K))]$	3440	K

### Module Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Isolation Voltage	V <sub>ISO</sub>	4.2	-	-	kV	RMS, f = 0Hz, t = 1s
Terminal RMS Current	I <sub>IRMS</sub>	-	500	-	A	T <sub>F</sub> = 85 °C, T <sub>Cl</sub> = 105 °C
Terminal Creepage	d <sub>CREEPAGE</sub>	-	9.0	-	mm	To Heatsink/Terminal
Terminal Clearance	d <sub>CLEARANCE</sub>	-	4.5	-	mm	To Heatsink/Terminal
Comparative Tracking Index	CTI	200	-	-		
Terminal Screw:M5	M	3.0	-	5.0	N*m	
Mounting Screw:M4	M	1.80	-	2.20	N*m	
Screw PCB to frame	M	0.45	0.50	0.55	N*m	
Weight	G	-	305	-	g	



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## Application Characteristics

### GaN Gate Drive

- GaN E-mode Gate Drive Voltage ( $V_{GS}$ ) is nominally -3V to +6.0V for high-power systems, to achieve optimal  $R_{DS(on)}$  performance and lifetime reliability. Absolute maximum  $V_{GS}$  rating is +7.0V (DC voltage), but GaN E-modes are rated for transients up to +10V and -20V, for pulses up to 1 $\mu$ s.
- Gate and commutation loop inductances are minimized in the module design (i.e., DBC layout and Pin configuration), however, wire-bonded case-type power modules will have higher loop inductances than embedded power modules with integrated gate drive. Therefore, careful gate driver board design must be implemented.

### GaN Reverse Conduction

- GaN E-modes do not have a parasitic body diode or a parasitic Bi-polar in their substrate, therefore the GaN E-mode has zero  $Q_{RR}$  and extremely high  $dV/dt$  ruggedness. But despite not having a body diode, the GaN E-mode will *inherently* conduct in reverse current flow (source-to-drain) through the 2DEG channel, when source-to-drain potential ( $V_{SD}$ ) is greater than  $V_{TH}$  (*approximately* 1.7V).
- During reverse conduction,  $V_{GS}$  can be zero volts (no gate bias is required for reverse conduction operation), and anti-parallel diodes are **not** required for reverse conduction.
- For optimal efficiency, dead time should be minimized and synchronous rectification should be implemented in the system design.

### GaN Blocking Voltage

- GaN E-mode blocking voltage ( $V_{(BL)DSS}$ ) is defined by the value of drain leakage Current ( $I_{DSS}$ ). Hard breakdown (unrecoverable) will occur well above the rated  $V_{(BL)DSS}$  value, similar to hard breakdown in a Si MOSFET or IGBT. As a general practice, the applied drain voltage should be de-rated in a similar manner as Si MOSFET or IGBT.
- All GaN power transistors do not avalanche and thus do not have an avalanche breakdown rating.
- The maximum drain-to-source rating does not change if negative gate voltage is applied.

### HybridPACK™ module case modification

- Additional pins were added along the centerline of each half-bridge portion, to connect to gate and source sense nodes for each GaN device in the half-bridge. Two 150A GaN transistors are paralleled for high-side and low-side switches, providing 300A current. The additional gate and source sense pins allow a symmetric DBC Layout and GaN device placement.

## Test Results

### Double Pulse Test (GS-EVx-3PH-650V300A-SM1x)

- Test Condition:  $V_{DS} = 400V$ ,  $I_D = 300A$ ,  $R_{g-ON} = 12\Omega$ ,  $R_{g-OFF} = 7\Omega$

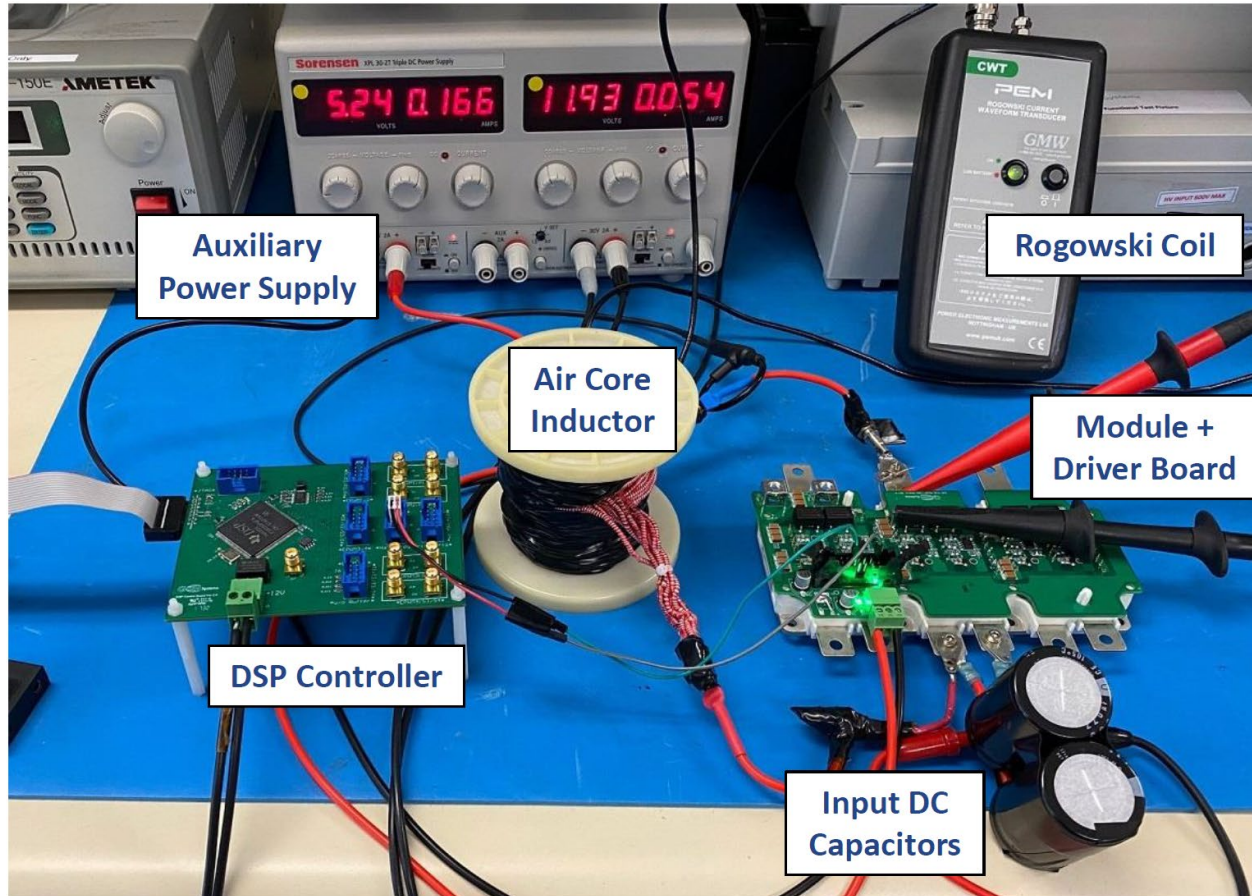


Figure 6 Double pulse test setup

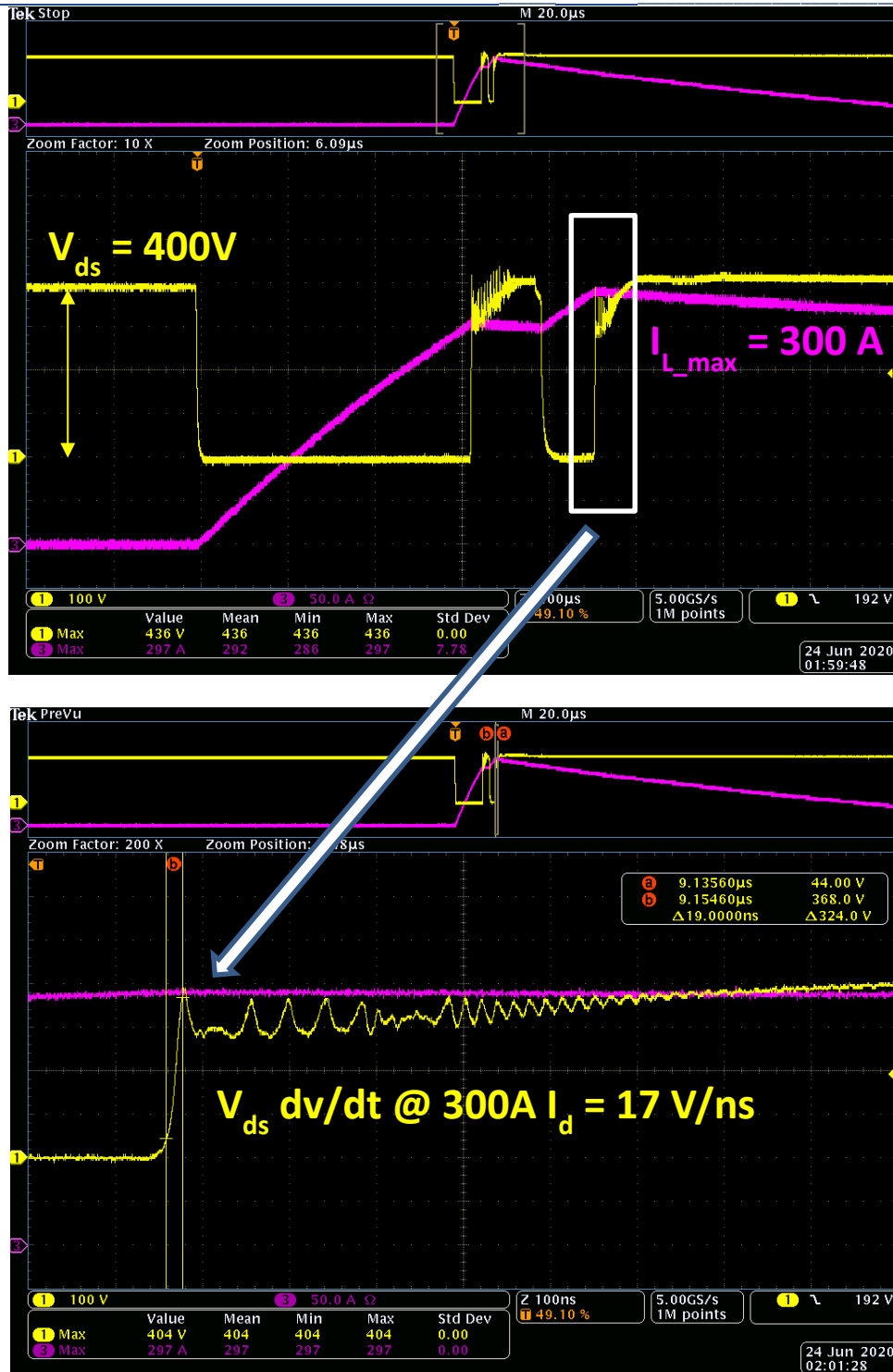


Figure 7 Double pulse test – Low Side GaN Switching OFF waveforms

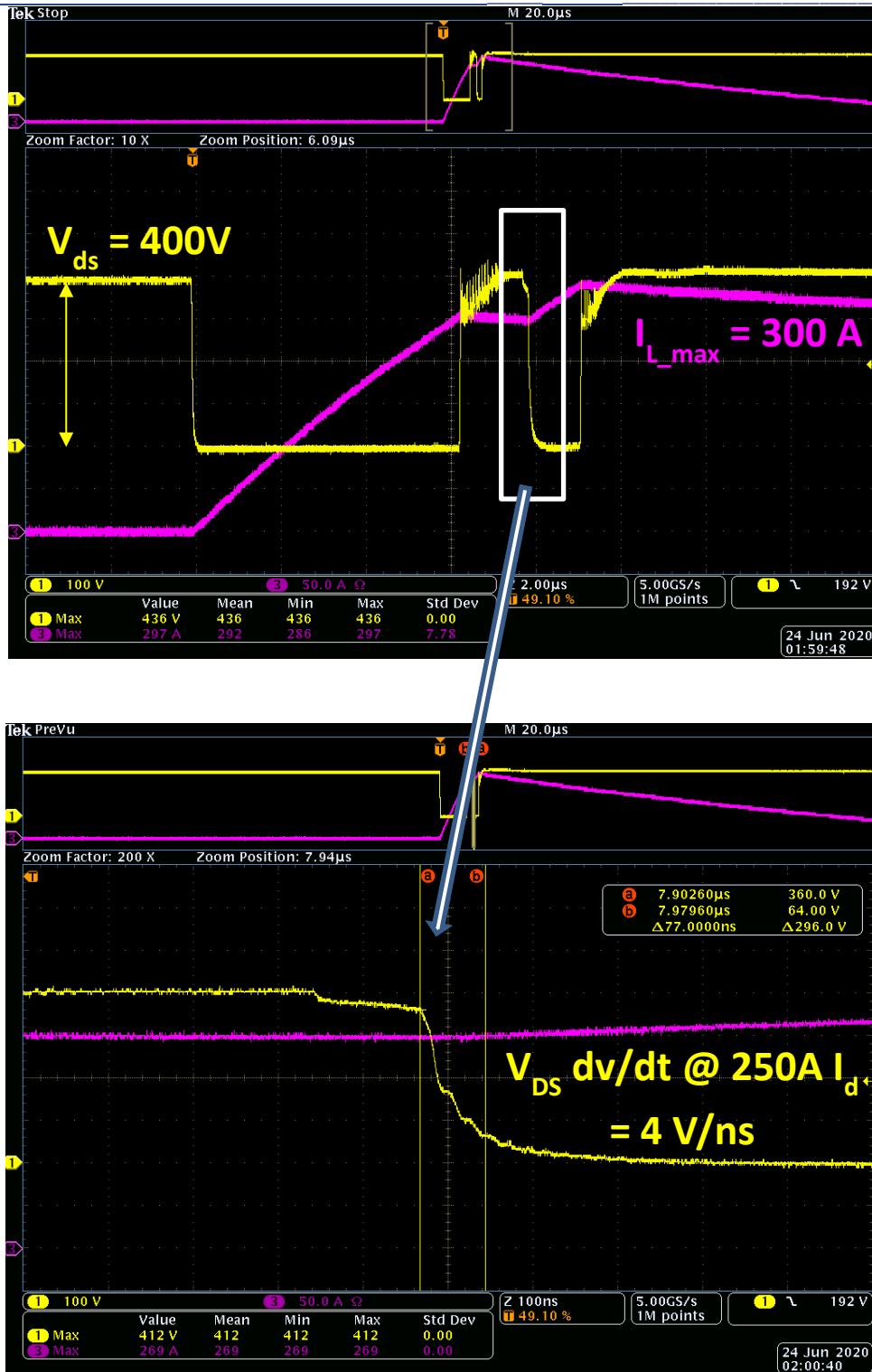


Figure 8 Double pulse test – Low Side GaN Switching ON waveforms

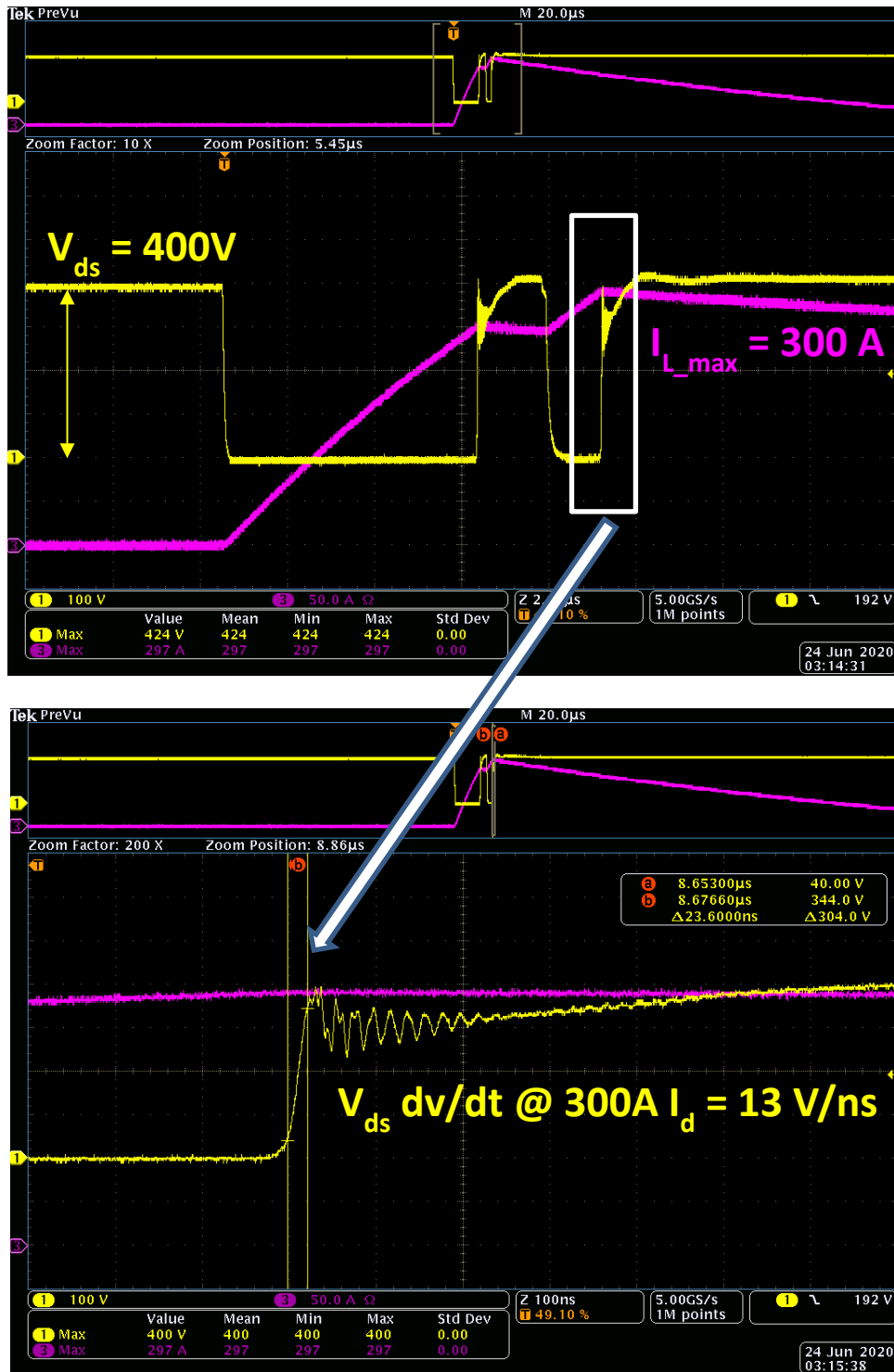


Figure 9 Double pulse test – High Side GaN Switching OFF waveforms

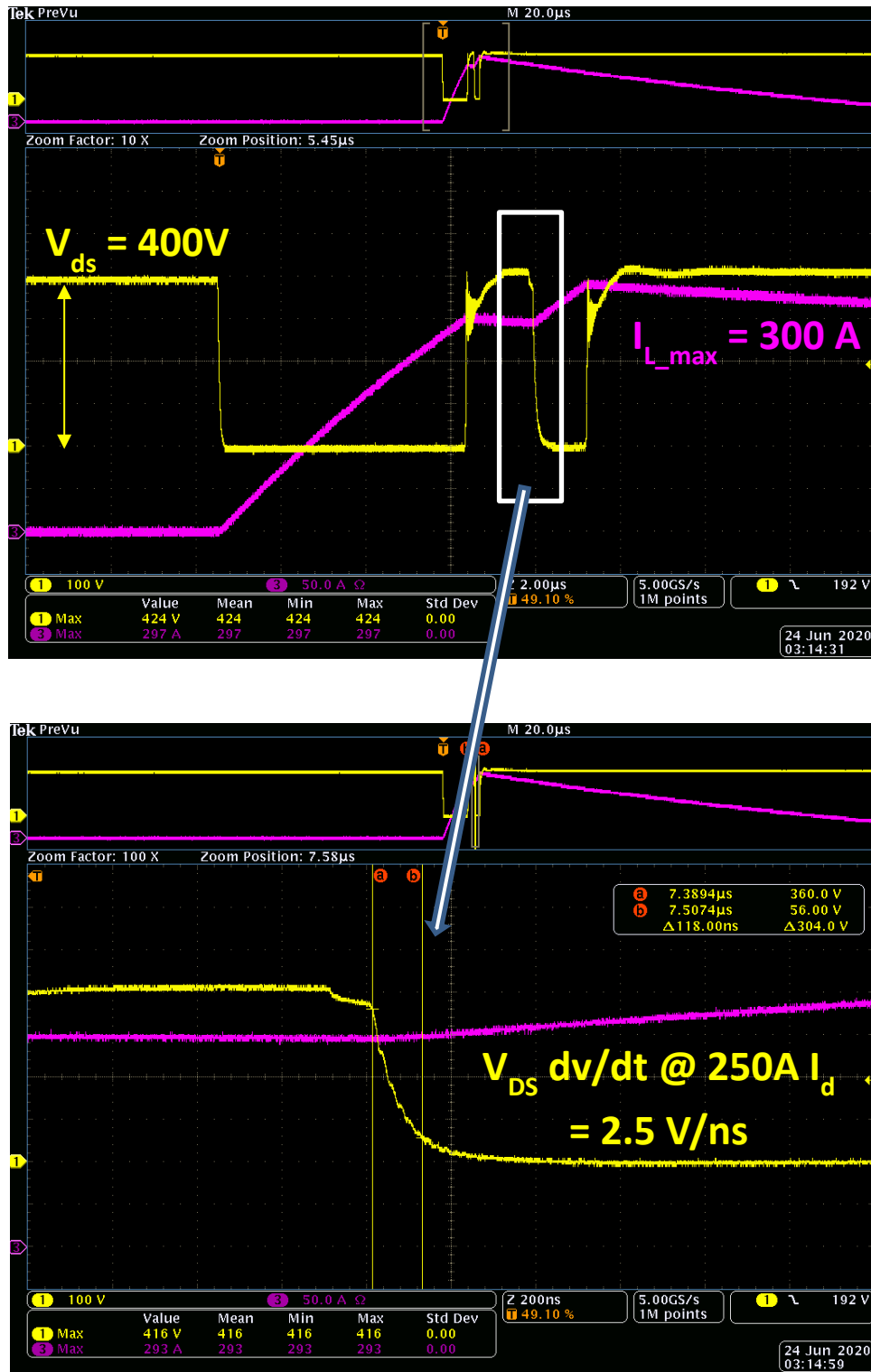


Figure 10 Double pulse test – High Side GaN Switching ON waveforms

## Mechanical Drawing

### Power Module

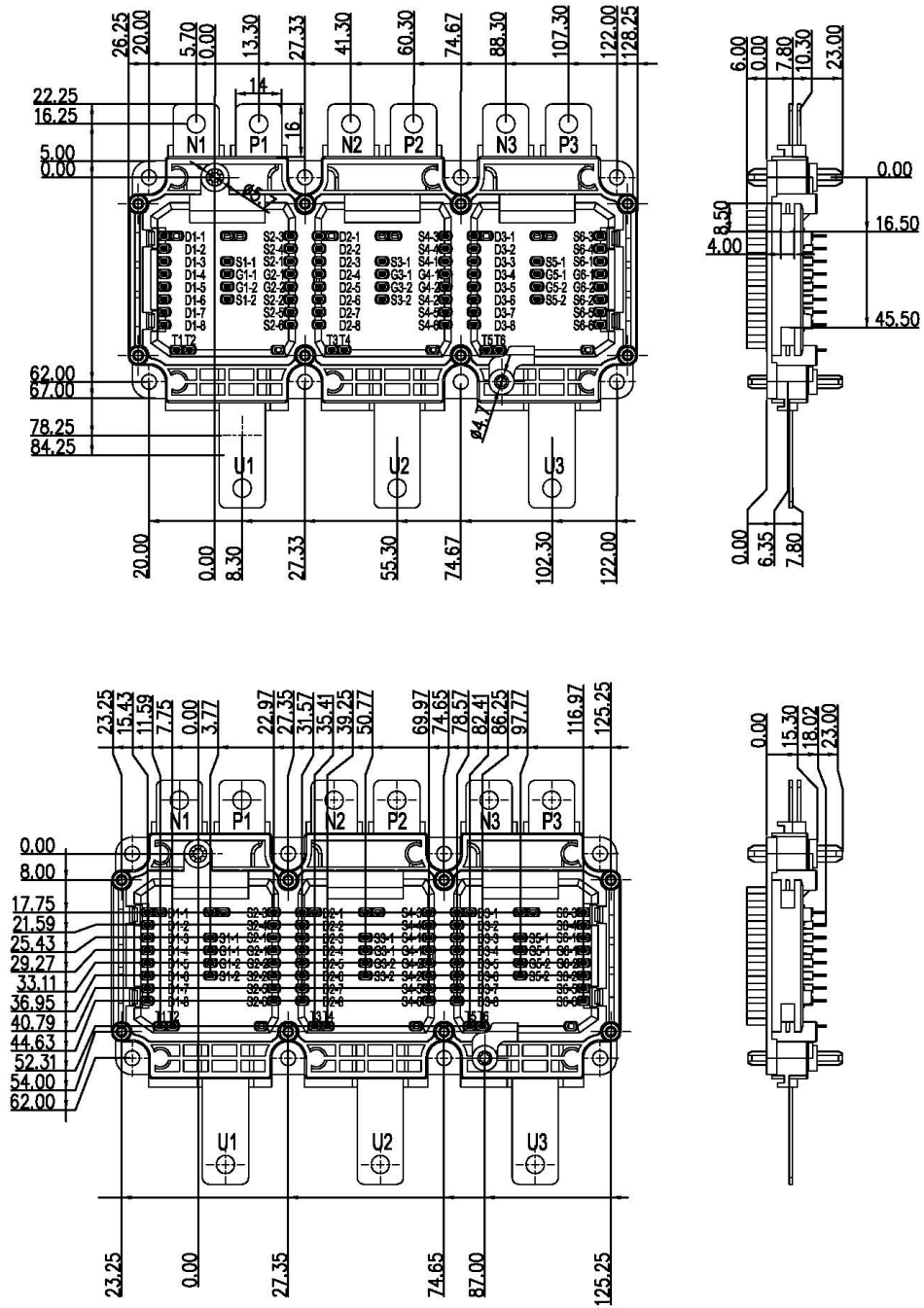


Figure 11 650V 300A GaN 3 phase Power Module Package Outline

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In Canada:

GaN Systems Inc.  
1145 Innovation Drive Suite 101  
Ottawa, Ontario, Canada K2K 3G8  
T +1 613-686-1996

In Europe:

GaN Systems Ltd., German Branch  
Terminalstrasse Mitte 18,  
85356 München, Germany  
T +49 (0) 8165 9822 7260

In the United States:

GaN Systems Corp.  
2723 South State Street, Suite 150,  
Ann Arbor, MI. USA 48104  
T +1 248-609-7643

[www.gansystems.com](http://www.gansystems.com)

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